Final Report

on

METAL-OXIDE SEMICONDUCTOR STABILITY STUDIES CAPACITANCE-VOLTAGE MEASUREMENTS

Contract No. NAS 5-3758
Procurement No. 670-W46755
Westinghouse G.O. 51248ATA

Prepared by

WESTINGHOUSE DEFENSE AND SPACE CENTER
Aerospace Division
Solid State Technology Laboratory
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GODDARD SPACE FLIGHT CENTER
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ABSTRACT

1992

A major objective of this investigation was to establish a comprehensive technique for the determination of the metal oxide semiconductor (MOS) device properties significant in a study of instability. A consideration of metal-oxide semiconductor theory determined that the voltage-dependent capacitance curves associated with these structures provide a wealth of information about their electrophysical properties and can readily be used for detecting and analyzing instability.

Two different but complementary approaches were developed for monitoring these capacitance-voltage curves. A capacitor-admittance technique establishes the quality of the device under study and particularly reveals those characteristics determined by the properties of the oxide layer. A frequency-determination technique, on the other hand, provides precise and detailed data well suited for analytical study and allows for interpretation of the effects of the various design parameters.

Equipment was established for the realization of both of these techniques, and data was compiled for a set of three p-channel units. Instability was effectively monitored by this method. Moreover, the data relates instability to the redistribution of charge in the oxide and also provides a means of determining the degree of this redistribution. Furthermore, irregularities such as carrier traps in the oxide can also be monitored. This approach therefore constitutes an efficient and effective tool for studying metal oxide semiconductor structures and can be used in the correlation of the design parameters with the electrical characteristics.

Author

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1. INTRODUCTION

The importance of the metal-oxide semiconductor (MOS) field effect transistor is increasing in solid state circuitry. Its unique properties of extremely high dc input impedance and pentode-like characteristics combine with the high reliability inherent in solid state devices to offer still another working tool in the design of molecular circuits. Because of these important practical applications, considerable effort is being directed to the study of the basic properties of MOS devices. Perhaps the major effort is an investigation of device stability.

MOS devices are susceptible to instability due to the presence of surface state charges which are mobile under conditions of temperature-bias stress. A thorough investigation in this regard should therefore monitor the presence of these charges which are the cause of instability rather than merely detect the change in turn of voltage which is a consequence of their redistribution. With this approach significant information can be gained into the nature of instability, and steps can more readily be taken to control or correct the factors which cause it. The surface state charge may be monitored through the use of the voltage-dependent capacitance curves. This technique is important not only because of the amount of pertinent information that it furnishes but also because of its efficiency and relative simplicity. For these reasons this method was adopted for use in this investigation of MOS structures.

2. SIGNIFICANCE OF CAPACITANCE-VOLTAGE CURVES

The distribution of charge at the oxide-silicon interface of a metal-oxide semiconductor (MOS) device is strongly dependent upon the applied bias. Figure 1 depicts the characteristic carrier states associated with these structures and also denotes the polarity necessary to induce these states in both p-channel and n-channel units. Where the device is forward-biased (positive on the gate of a p-channel unit), majority carriers accumulate at the silicon surface so that the semiconductor is much like a metal. In this case the capacitance of the MOS structure is approximated by the capacity of the oxide layer alone. As the bias is reduced to zero and slightly in the reverse direction, the majority carriers are depleted from the vicinity of the semiconductor surface, and the uncompensated impurity ions then govern in this region. Since this depletion region, in effect, adds to the thickness of the dielectric, the capacitance decreases. With stronger back bias, minority carriers are attracted to the vicinity of the interface. These form a narrow inversion channel the polarity of which gives name to the device. If the minority carriers are sufficiently mobile to respond to the excitation signal, the capacitance in this region will again be increased as is shown by the dashed curve in figure 2. This figure depicts the typical capacitance associated with a device and also defines the three surface conditions of charge accumulation, depletion and inversion.

The distribution of charge at the silicon surface is influenced by conditions of processing. However, for any individual unit, variation of the applied gate voltage induces states of accumulation, depletion or inversion. It is to be expected, therefore, that the capacitance exhibited by the device will differ as a consequence of the different mobilities and recombination times associated with each of these carrier states.

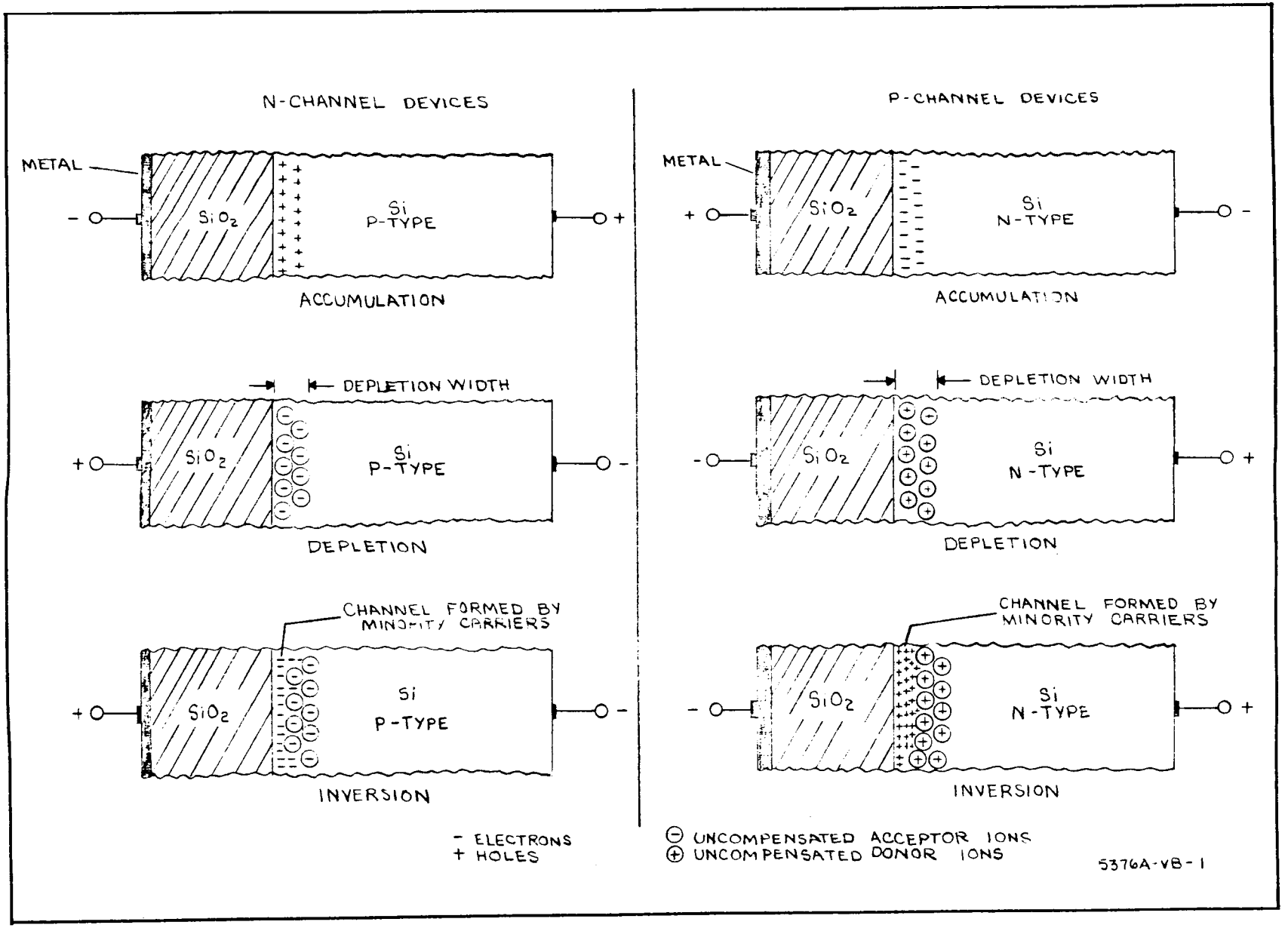
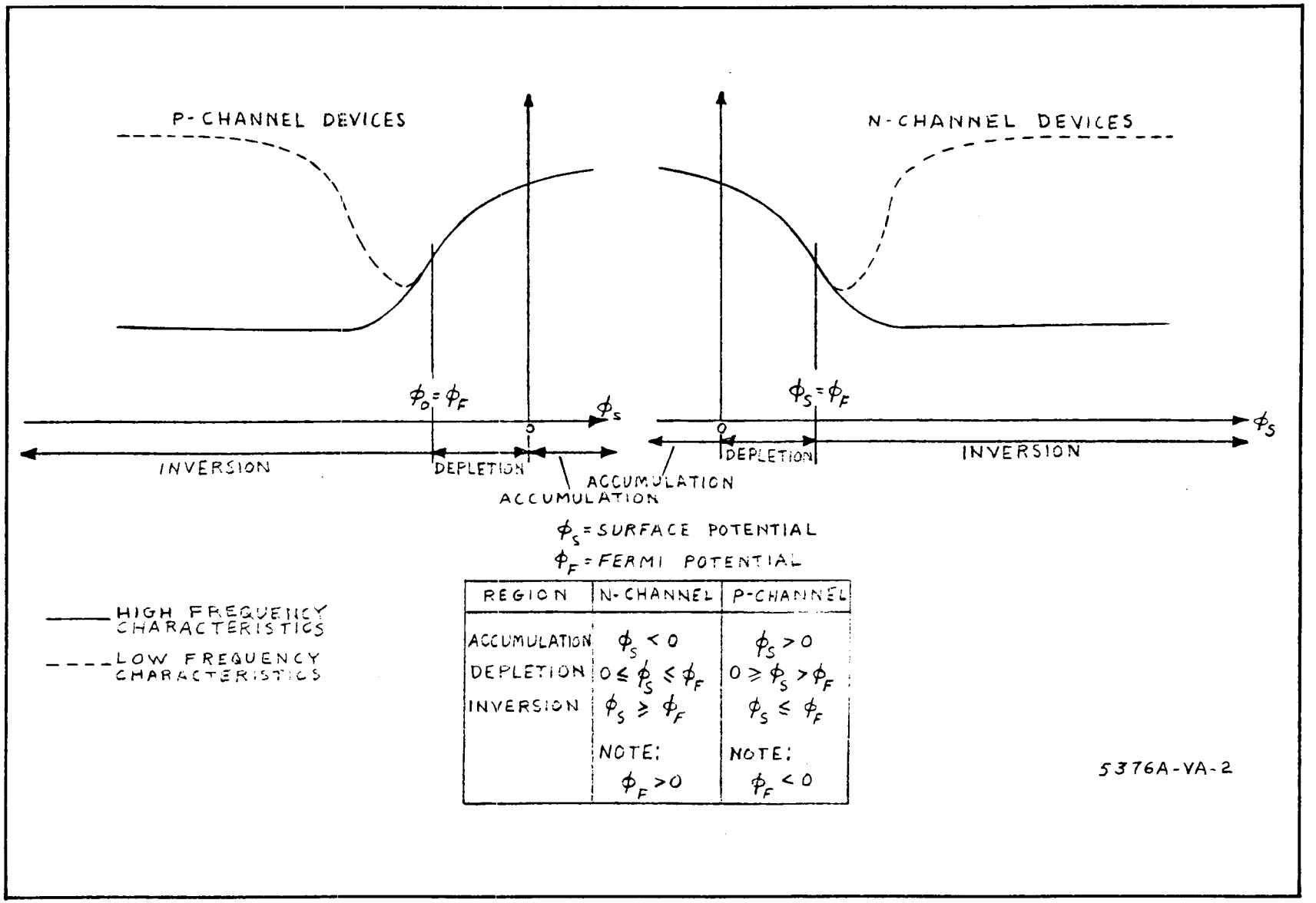


Figure 1. Surface Charge in MOS Devices



REGION	N-CHANNEL	P-CHANNEL
ACCUMULATION	$\phi_s < 0$	$\phi_s > 0$
DEPLETION	$0 \leq \phi_s \leq \phi_F$	$0 \geq \phi_s > \phi_F$
INVERSION	$\phi_s \geq \phi_F$	$\phi_s \leq \phi_F$
	NOTE: $\phi_F > 0$	NOTE: $\phi_F < 0$

Figure 2. Capacitance Characteristics Defined for the Three Distributions of Carrier States

In this regard the capacitance associated with the inversion state is most susceptible. At sufficiently high frequencies the minority carriers are not capable of responding to the variations in the excitation signal, and the capacitance shows little, if any, detectable reaction to further changes in applied voltage. At lower frequencies the minority carriers do have sufficient reaction time to respond to the excitation signal, and the corresponding capacitance then indicates the effect of the inversion charges. It is to be noted that the low-frequency mode may be realized other than by resorting to an actual reduction in the frequency of the measurement signal. This is accomplished by connecting the source (of an MOS transistor) to the body (bulk) of the semiconductor, thereby providing a rapid equilibration path for the inversion charges. The distinction between high and low frequency modes of operation is not abrupt, however, and at any specific frequency the degree to which a particular device exhibits the characteristics of either mode is dependent upon the physical design parameters.

The capacitance (C) of an MOS structure is a series composite of the capacitance of the oxide layer (C_o) and the capacitance of the space charge region (C_s). Since the capacity of the oxide layer is fixed by its physical dimensions, the variations in the device capacitance correspond to the changes in the capacity of the space charge region. For the high-frequency mode this is given by the relation[1]

$$C_s = K_s \epsilon_o / x_d \qquad (1)$$

where C_s in the capacitance per unit area of the space charge region, K_s is the dielectric constant of the semiconductor, ϵ_o is the permittivity of free space, and x_d is the effective width of the depletion region. This capacity is seen to be unaffected by the inversion charges and is relatively constant, varying only according to the small-scale changes in the effective depletion width.

1. A.S. Groove, et al, "Investigation of Thermally Oxidized Silicon Surfaces Using Metal-Oxide-Semiconductor Structures," Solid State Electronics, Vol. 8, No. 2 (February 1965).

The space charge capacitance associated with the low frequency mode is governed by the relation[2]

$$C_s = K_s \epsilon_o \frac{q \rho_s}{Q_s} \tag{2}$$

where

$$\rho_s = p_s - n_s + N_D - N_A \tag{3}$$

and

$$Q_s = -2 \frac{\phi_s}{|\phi_s|} q n_i \left[\frac{kT}{q} \frac{K_s \epsilon_o}{2q n_i}\right]^{1/2} \left\{2 \cosh \frac{q}{kT} (\phi_s - \phi_F) - \cosh \frac{q}{kT} \phi_F + \frac{q}{kT} \phi_s \sinh \frac{q}{kT} \phi_F\right\}^{1/2} \tag{4}$$

where

q = magnitude of electronic charge

ρ_s = surface charge concentration

n_i = intrinsic carrier concentration of the semiconductor

n_s = electron concentration at the surface

p_s = hole concentration at the surface

N_D = donor ion concentration

N_A = acceptor ion concentration

ϕ_F = Fermi potential of the semiconductor

ϕ_s = surface potential

Q_s = total charge in the semiconductor

k = Boltzmann's constant

T = absolute temperature

This expression for C_s is seen to depend on the charge concentration and will specifically reflect the changes caused by the inversion charges.

Figure 2 depicts typical capacitance-voltage curves for both p- and n-channel units and indicates the regions governed by each of the three carrier states. The difference in the displays obtained through low- and high-frequency modes of operation is also shown. Since the inversion region begins

2. Ibid.

at the point where $\phi_s = \phi_F$, this point defines the turn-on voltage of the unit. The surface potential, however, is not readily detectable under experimental conditions but may be established through the following expression:[3]

$$\phi_s = V_g - \phi_w + \frac{1}{C_o}\left[Q_{ss} + Q_s\right] \tag{5}$$

where V_g is the applied gate voltage, ϕ_w is the metal-semiconductor work function, C_o is the oxide capacitance per unit area, Q_{ss} is the charge associated with the surface states, and Q_s is the space charge given by equation 4. This expression may then be evaluated if the surface state charge can be determined.

In this regard the capacitance-voltage curves are most advantageous. The surface state charges associated with a particular type of device can be determined by a comparison of the capacitance-voltage curves obtained through experiment with those expected for the device on the basis of semiconductor equilibrium theory. The effect of the surface state charge is indicated as a horizontal (voltage) shift of the experimental curve with reference to the theoretical curve. The exact relation is depicted in figure 3. The magnitude of the shift is given as

$$\frac{Q_{ss}}{C_o} - \phi_w,$$

but since both ϕ_w and C_o are determined from design considerations, this shift determines the value of the surface state charge. It should be noted that the above relations allow the use of the capacitance-voltage curves to evaluate and control the processing techniques, and further, to correlate the design parameters with the electronic characteristics of the device.

The voltage-dependent capacitance curves thus not only provide an electrophysical profile of the device but also are especially well suited to the study of stability because they enable monitoring of the surface state

3. Ibid; and C. T. Sah, "Characteristics of the Metal-Oxide-Semiconductor Transistors," IEEE Transactions on Electron Devices, (July 1964).

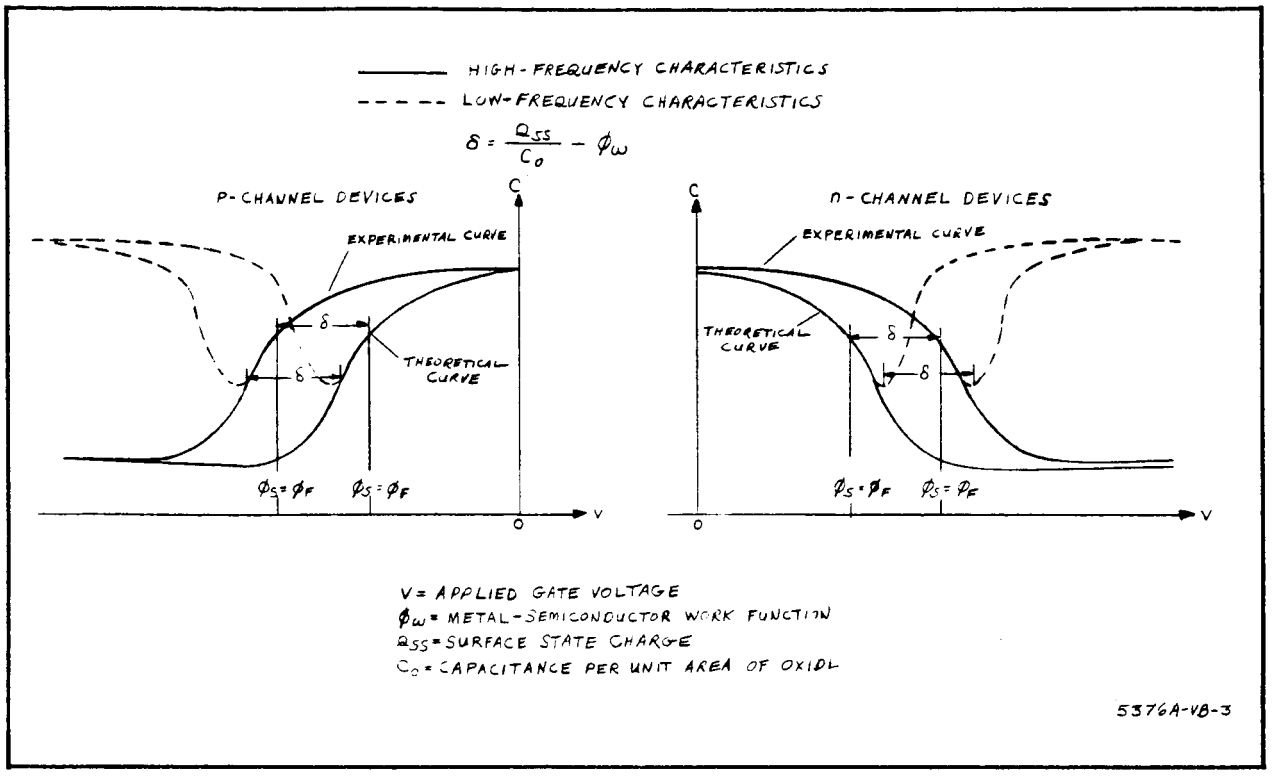


Figure 3. Effect of Surface State Charge on the Voltage-Dependent Capacitance Curves

phenomena. This method, like the ordinary conductance technique, gives an indication of the variation in turn-on voltage; but of much more importance, it also reveals the properties of the oxide layer. The character of the oxide is known to strongly influence the stability of MOS units.

The space charge on the silicon surface is always balanced by a net external charge of opposite polarity. The external charge, however, may be composed of any surface state charge in the oxide and interface as well as the charges introduced on the metal electrode. Since the behavior of these surface states affects the electric field in the vicinity of the conductance channel, their influence on the turn-on voltage is considerable. Moreover, due to the ability of these charges to redistribute under certain environmental conditions, their presence will be a major cause of device instability. The redistribution of these charges however may be monitored through the use

of capacitance-voltage measurements. Specifically, conditions tending to vary the surface state charge concentration in the oxide near the oxide-semiconductor interface will tend to shift the capacitance-voltage characteristics along the voltage axis. The creation of charge in the interface, on the other hand, tends to extend (along the voltage axis) the transition between plateaus on the capacitance-voltage curves.

The theoretical calculations given previously are expressed in terms of physical design parameters and can be used to arrive at a quantitative description of the charge states of the MOS system. For device stability studies, however, interest is centered not so much on the actual quantity of this charge as on whether it changes after exposure to various environmental conditions. Thus, for any particular unit it is necessary only to monitor the position of the capacitance-voltage characteristics with respect to the initial room-temperature curve. This room-temperature characteristic then supersedes the theoretical curve in the previous considerations. The variations in the turn-on voltage may also readily be observed by monitoring the shift of the capacitance minimum. This point is more clearly defined than the point where $\phi_s = \phi_F$ but shifts in direct relation to it. Moreover, the choice of this point in effect redefines the turn-on voltage at a greater value of reference current. With these modifications in the procedures, the parameters associated with device stability can be studied without the necessity for repeated calculations based on involved physical parameters.

3. APPARATUS AND EXPERIMENTAL MEASUREMENTS

Two approaches were used to determine the voltage-dependent capacitance characteristics. The first depends upon the admittance properties of a capacitor and is used primarily for a qualitative determination of the device characteristics. The second method, which is based on frequency monitoring, is more suitable for quantitative study.

3.1 CAPACITOR CONDUCTANCE METHOD

In the admittance-oriented technique, the test sample is driven by a signal of constant amplitude and fixed frequency while simultaneously being swept through a selective range of dc bias. The ac current through the sample is monitored and displayed on an oscilloscope along with an indication of the instantaneous dc bias. Since the current is a function of the capacity, this, in effect, gives a capacitance-voltage display. The circuit employed for this technique is shown in figure 4.

In this figure E_g represents an audio signal generator and E_s is a ramp function voltage used for biasing the test sample (C_1). The resistor (R_1) is used as a readout for the current flowing through the test sample. The impedance branches Z_2 and Z_3 comprise a voltage divider for the signal supplied by E_g. The test signal (E_T) established by this divider will be fixed in amplitude if Z_2 is much less than Z_1. Then, omitting the voltage biasing section, the above circuit reduces to the simple equivalent given in figure 5.

From this figure, the current flowing through the test sample is readily determined to be

$$I_1 = \left(\frac{j\omega}{j\omega + \frac{1}{R_1 C_1}} \right) I_T \qquad (6)$$

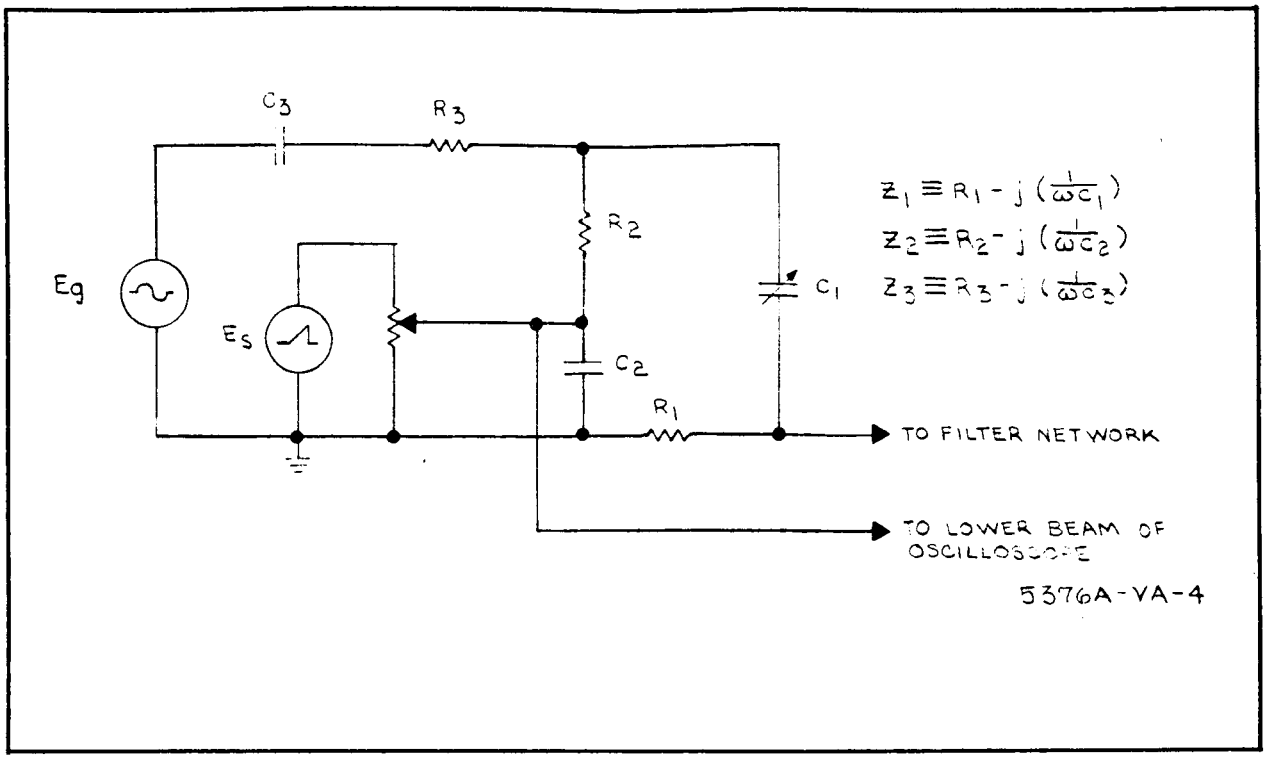


Figure 4. Circuit Diagram for Admittance Method of Capacitance Detection

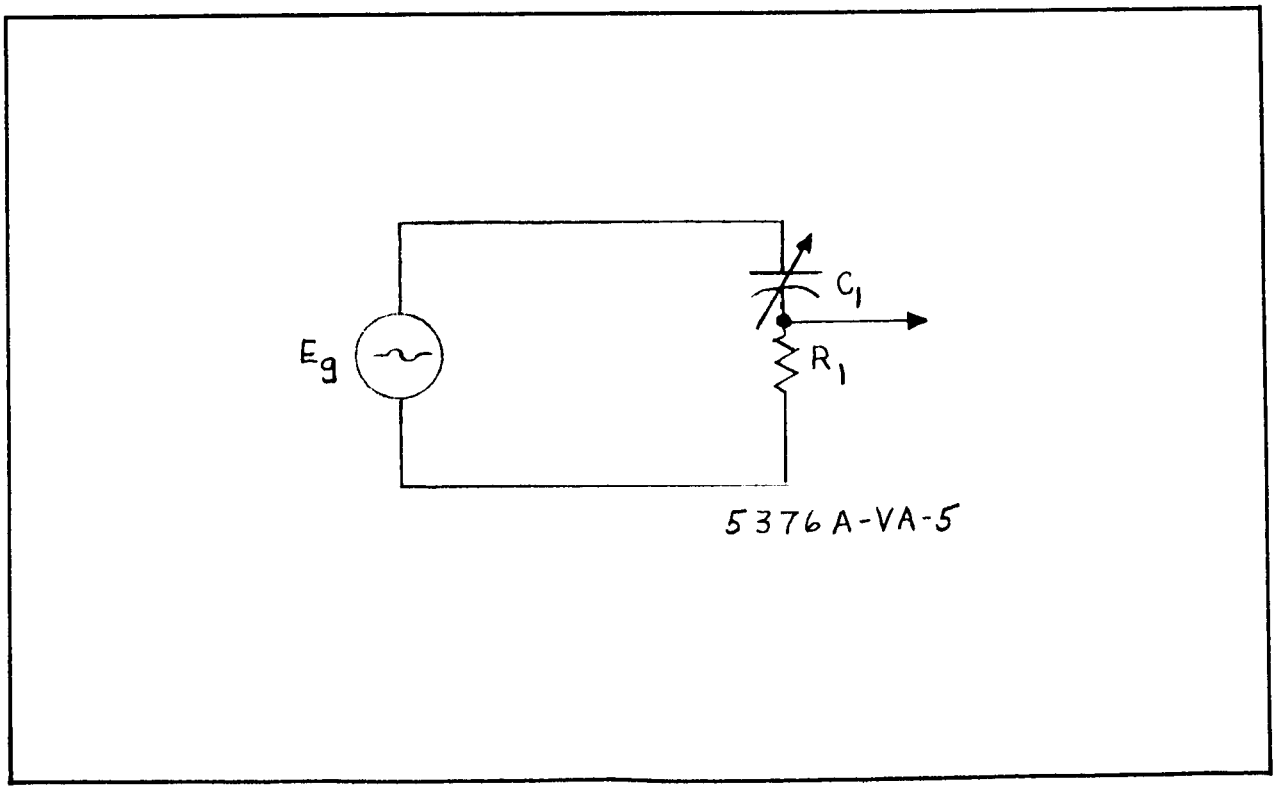


Figure 5. Basic Equivalent Circuit

where I_T, defined as E_T/R_1, is the current which would flow if the test sample were shorted. The coefficient of attenuation

$$\left[\alpha \equiv \left| \frac{I_1}{I_T} \right| \right]$$

is then established as

$$\alpha = \frac{\omega R_1 C_1}{\sqrt{1 + (\omega R_1 C_1)^2}} \tag{7}$$

and if $\omega R_1 C_1 << 1$, this reduces to

$$\alpha \cong \omega R_1 C_1 \tag{8}$$

This condition, and the fact that ω and R_1 are both fixed in value, establishes a unique and direct interdependence between I_1 and C_1. Therefore the capacitance can be determined by monitoring the current.

However, a lower limit on the magnitude of R_1 exists because the output voltage is monitored across this resistor, and the signal must be kept above the surrounding noise level. Further limitation is imposed by the fact that the test voltage established by the voltage divider must be kept small enough not to affect the bias level on the test unit. A compromise in the design must therefore be made dependent upon the expected magnitude of the capacitance to be measured and upon the sensitivity of the apparatus available for the isolation and detection of the output signal. The operating frequency is also chosen in consideration of these criteria. The bias voltage is obtained from a sawtooth generator having the provisions for adjustment of slope and repetition rate.

The following parameters and equipment were selected for the testing apparatus.

R_1 = 100 kilohms

R_2 = 10 ohms

R_3 = 1 kilohm

C_2 = 1000 picofarads

C_3 = 10 picofarads

Oscilloscope - Tektronix Model No. 551 with plug-in units Type E and Type Z.

E_S = sawtooth signal available from the oscilloscope attenuated to the desired amplitude by a 50-kilohm potentiometer. Maximum available amplitude = 150 volts repetition rate = 50 msec.

E_S = Audio Oscillator - Hewlett-Packard Model 200 CD

Operating frequency (f_o) = 20 kc

Test signal (E_T) = 50 mv

These values were derived through the following considerations.

The maximum capacitance of the test units was expected to be about 20 picofarads. The most sensitive plug-in unit for the Tektronix oscilloscope, the Type E Differential Amplifier, is capable of detecting low-level signals at a maximum frequency of 20 kc. The sensitivity corresponding to this bandwidth is 0.05 millivolts. To take advantage of this sensitivity, a testing frequency of 20 kc was chosen. At this frequency a 20 picofarad capacitor exhibits a 400 kilohms impedance. As a compromise to satisfy the criteria stated previously, R_1 was chosen to be 100 kilohms. The voltage divider consisting of Z_2 and Z_3 was designed to provide a test signal E_T sufficiently small as not to influence the bias of the test unit. To keep this signal constant in amplitude, Z_2 had to be a much smaller impedance than Z_1 for all values of C_1. To ensure this for all conditions, Z_2 was made smaller than R_1. With the component values given before, the attenuation of the voltage divider was set at 100 so that a 5-volt signal had to be provided at the audio oscillator to obtain 50 millivolts for E_T. Moreover, with these component values, $\omega R_1 C_1 = 0.04$ for C_1 = 20 picofarads and decreases with reductions in C_1 (as occurs with increasing bias). This condition satisfies the design criterion that $\omega R_1 C_1$ be much less than 1 and establishes a maximum coefficient of attenuation $a_{max} = 0.04$. Under these conditions the output signal is 2 millivolts, emphasizing the need for a sufficiently large value of R_1.

The time-dependent nature of the voltage bias introduces an additional current through the test unit which must be eliminated from the display to obtain a meaningful capacitance measurement. This was accomplished through the use of the RC rolloff filter depicted in figure 6.

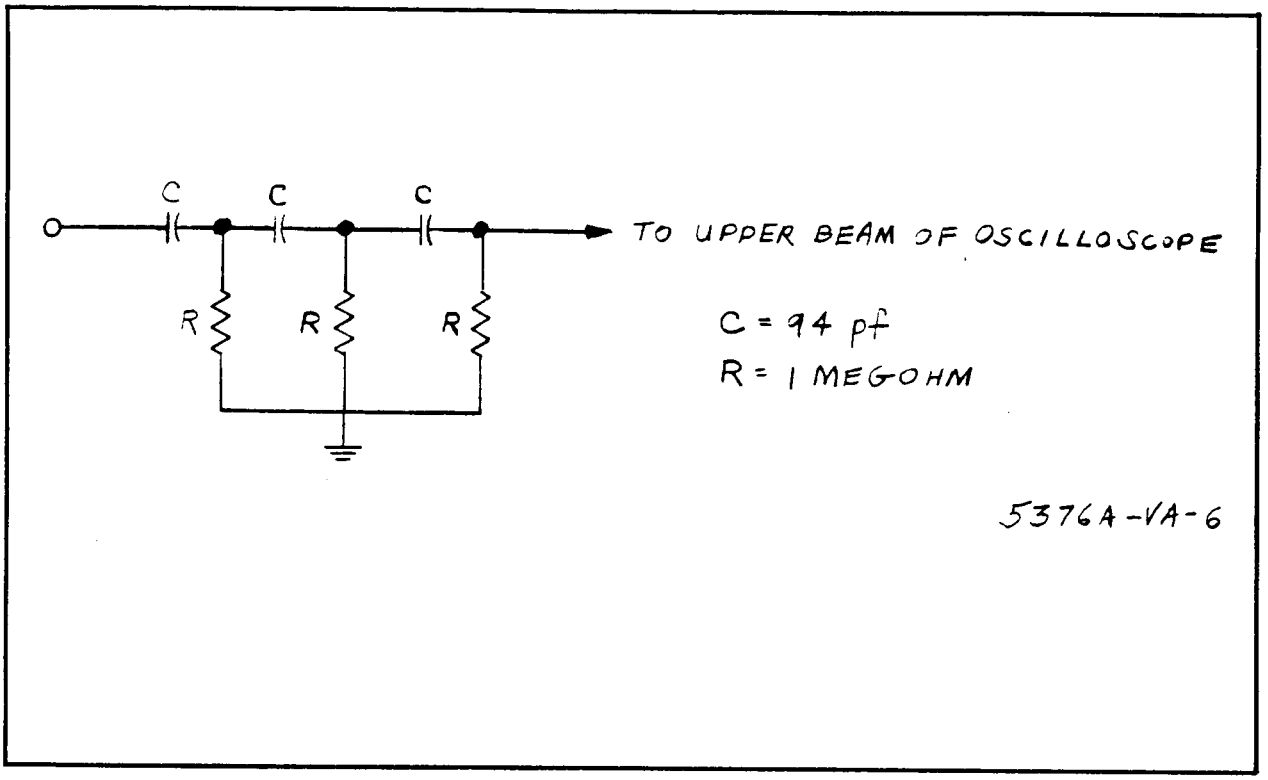
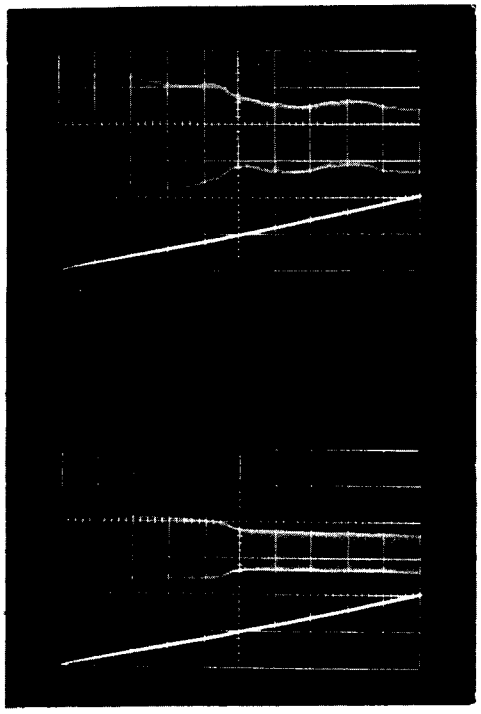


Figure 6. Filter Network

The coefficient of attenuation for the 20-kc signal through this filter is $a_f = 0.876$. Elimination of the low frequency currents associated with the repetition rate of the voltage bias is good. The displays obtained with and without the use of the filter are shown in figure 7. The filter represents a load that is equivalent to a series combination of a 337-kilohm resistor and a 62.5 picofarad capacitor. For the ideal case, both of these magnitudes should approach infinity.

The major advantage of this admittance-oriented technique is that it quickly and effectively allows a preliminary scan to determine the quality of the device being studied. Moreover, this technique readily makes evident such related



UPPER GRID: CAPACITANCE CHARACTERISTICS DISPLAYED WITHOUT FILTER

LOWER GRID: CAPACITANCE CHARACTERISTICS DISPLAYED WITH FILTER

SCALE
SWEEP 5 MSEC PER DIVISION
UPPER TRACE
UPPER GRID 2 MV PER DIVISION
LOWER GRID 1 MV PER DIVISION
LOWER TRACE 5V PER DIVISION

5376A-PF-7

Figure 7. Effects of Filter Network on Capacitance Display

information as leaky dielectric, breakdown voltage, and other associated phenomena which tend to obscure tube capacitance measurements. However, the use of this method is limited through restrictions imposed by extraneous noise. Moreover the small size of the display does not readily lend itself to quantitative analysis.

3.2 FREQUENCY DETECTION TECHNIQUE

The frequency detection technique employs the test sample (under a variable dc bias) as a branch of a variable oscillator. The signal from this oscillator is acted upon by a series of wave-shaping networks to give a voltage signal proportional to the change in frequency. This voltage is therefore characteristic of the capacitance and is recorded on an X-Y plotter. A block diagram for this technique is given in figure 8.

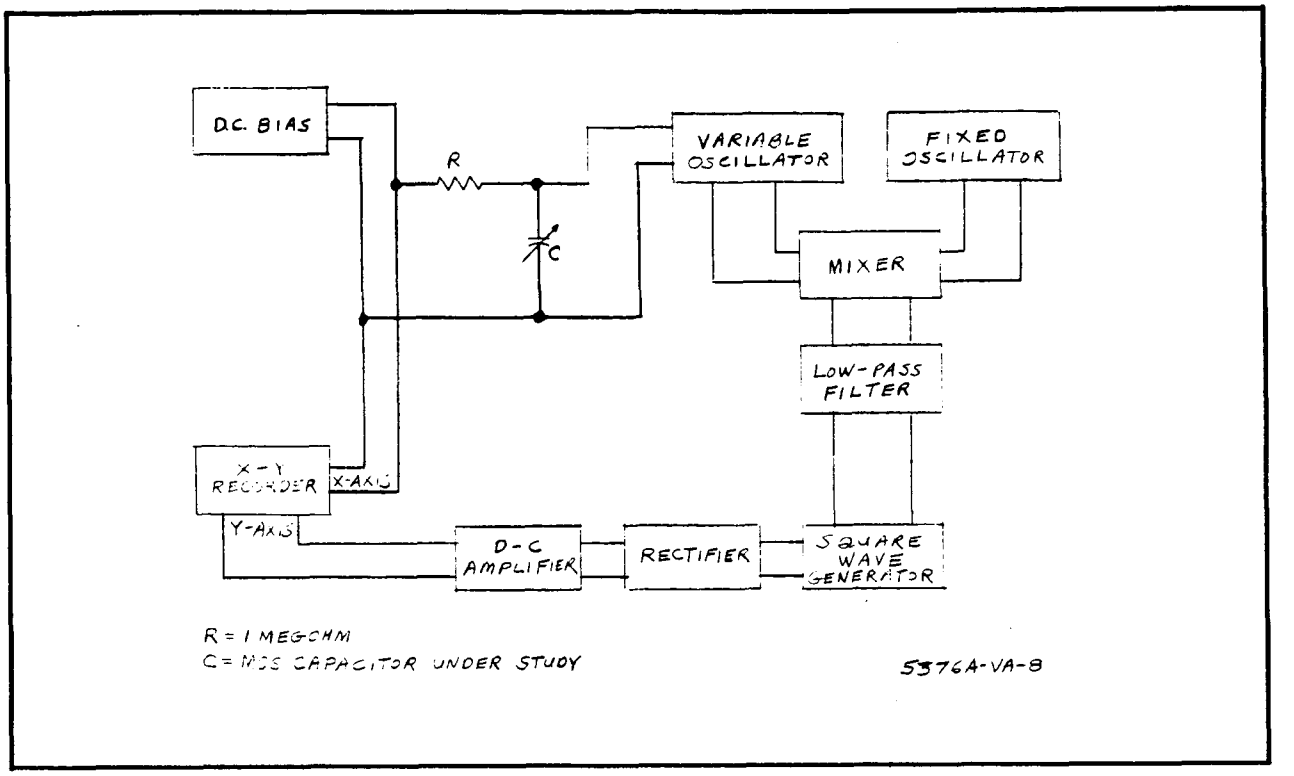


Figure 8. Block Diagram of Frequency Monitoring Method of Capacitance Detection

Operation depends upon using the MOS structure to regulate the frequency of a Colpitts oscillator. The signal from this oscillator is mixed together with one from the fixed frequency oscillator and subsequently filtered (low pass) to obtain an indication of the frequency change caused by the MOS unit. A square wave generator is then triggered by the output, and, after rectification, the resulting signal is an indication of the capacitance of the test sample. The equipment used to realize this configuration is as follows:

DC power supply	Hewlett-Packard Model 721 (0-30 volts)
Recorder	Moseley Autograph Model 3A
Ammeter	Hewlett-Packard Model 425A Microvoltammeter
L-C Meter	Tektronix Model 130

The Model 130 L-C meter and the Model 425A ammeter comprise the entire composite of the Y-axis network so that the equipment hookup is as shown in figure 9.

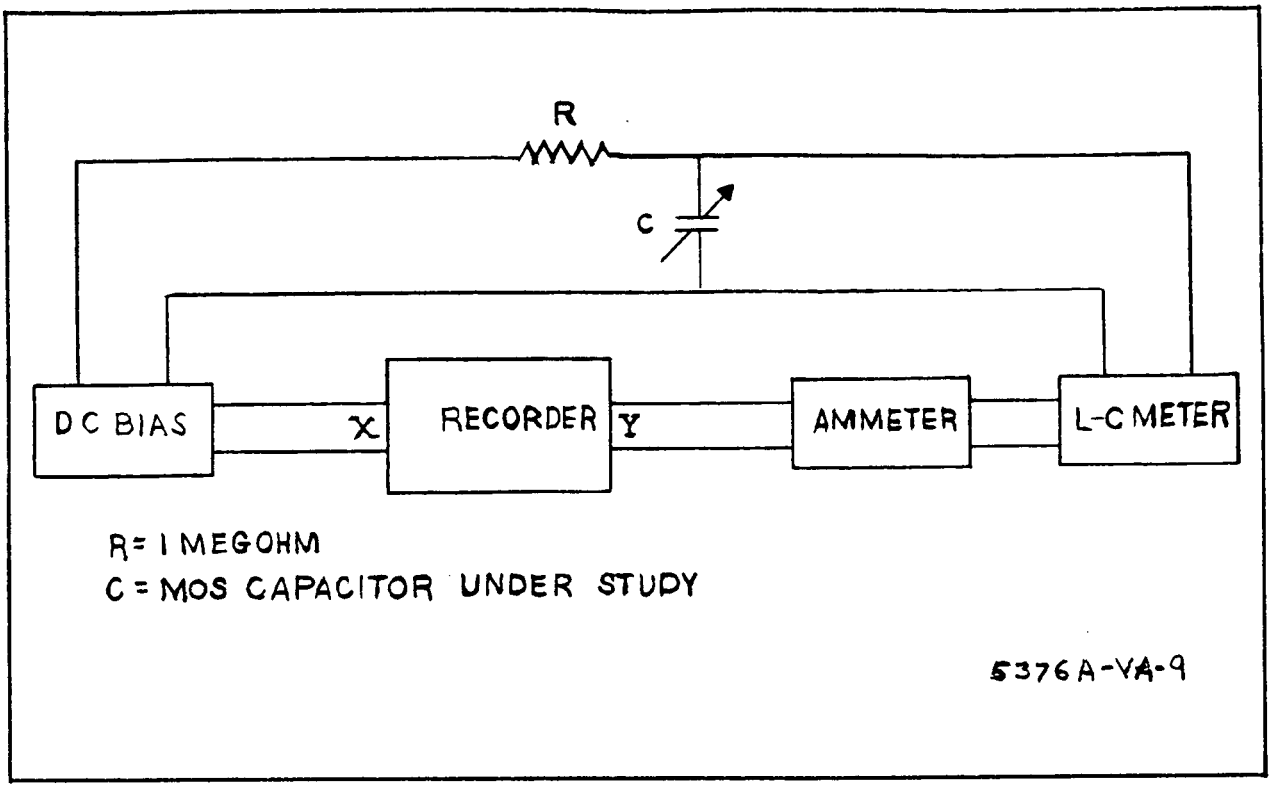


Figure 9. Connection of Equipment for Realization of Frequency Monitoring Technique

The following modifications in the equipment must be made. The L-C meter is not equipped with a set of output terminals. These are provided by cutting into one of the leads going to the display meter. The leads to the 425A ammeter bridge this gap. However, one of the leads to the ammeter is ordinarily grounded, and this ground must be removed before the ammeter leads are connected to the leads of the L-C meter. (These are 150 volts above ground.) The voltage output from the ammeter is connected to the ordinate of the recorder, which can be calibrated directly in terms of capacitance. Calibration is achieved by control of the potentiometer setting on the 425A ammeter and through adjustment of the gain settings on the X-Y recorder. Through proper calibration and with appropriate range settings, the apparatus is capable of performance resulting in a reproducibility to within 0.05 volts on the horizontal axis. The reproducibility on the vertical axis is within 1.5 percent of the full range value.

The major advantage of this method is that it provides a precise and detailed record of experimental data well suited for analytical study. Moreover, the apparatus employed for this technique can readily be adapted to record the turn-on voltage of the unit as monitored through the usual conductance detection method.

3.3 EXPERIMENTAL PROCEDURE

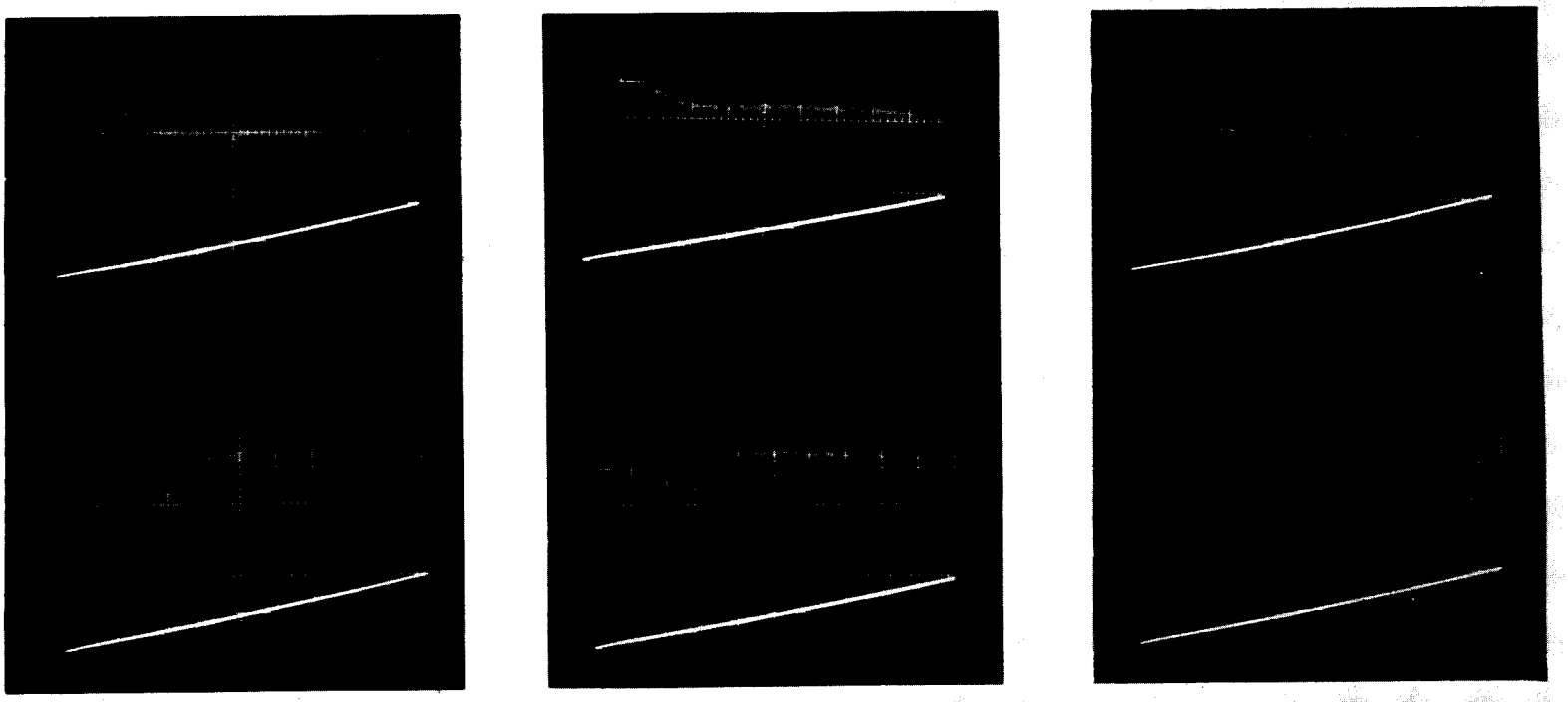
Stability data for p-channel devices was obtained by recording the characteristics of units subjected to three different environmental conditions.

1. Environment A - Off-the-shelf devices were initially tested at room temperature to obtain the typical characteristics of these structures. The resulting initial curves served as a basis of reference for subsequent data.

2. Environment B - The units were then subjected to a temperature of 150°C for 7 hours. The temperature of the units was then allowed to return to room temperature and data was again obtained.

3. Environment C - Finally the devices were biased in the reverse direction and held at 150°C for 16 hours. The units were then returned to room temperature, and a concluding set of data was taken.

For each of these sets of data the sequence of operation was as follows: A capacitance-voltage curve was first obtained by using the admittance technique. This gave an indication of the capacitance range for the device as well as indicating its quality. The frequency-monitoring technique was then used to obtain a detailed capacitance curve. Finally, the device conductance was plotted to achieve an indication of the turn-on voltage. This data for three different units is depicted in figures 10 through 30. The data is divided into three sets according to the unit being studied. Figures 10 through 16 pertain to the first unit, figures 17 through 23 to the second, and figures 24 through 30 to the third. The first figure of each sequence depicts the characteristic capacitance curves for that unit, subject to each of the three environmental conditions and detected through the admittance technique. All subsequent capacitance curves in a set were obtained by means of the frequency detection technique. The next two figures in a set depict respectively the capacitance characteristics and the conductive properties of the unit as obtained before it was subjected to any environmental stress conditions. The following two figures show the same properties after the device was subjected to the conditions of environment B, and the last two figures after subjection to environment C.



INITIAL ROOM TEMPERATURE CHARACTERISTICS

CHARACTERISTICS AFTER ENVIRONMENT OF 150° C FOR 7 HOURS

CHARACTERISTICS AFTER ENVIRONMENT OF 150° C WITH GATE VOLTAGE OF +30V FOR 16 HOURS

(SWEEP 5 MSEC PER DIVISION)

UPPER TRACE (VERTICAL SCALE 0.1 MV PER DIVISION)
UPPER GRID: CAPACITANCE FROM GATE TO BODY
LOWER GRID: CAPACITANCE FROM GATE TO BODY TIED TO SOURCE
LOWER TRACE (VERTICAL SCALE 5V PER DIVISION)
BIAS VOLTAGE DISPLAY

5376A-PF-10

Figure 10. Voltage-Dependent Capacitance Curves for Unit No. 1 - Detected by Admittance Technique

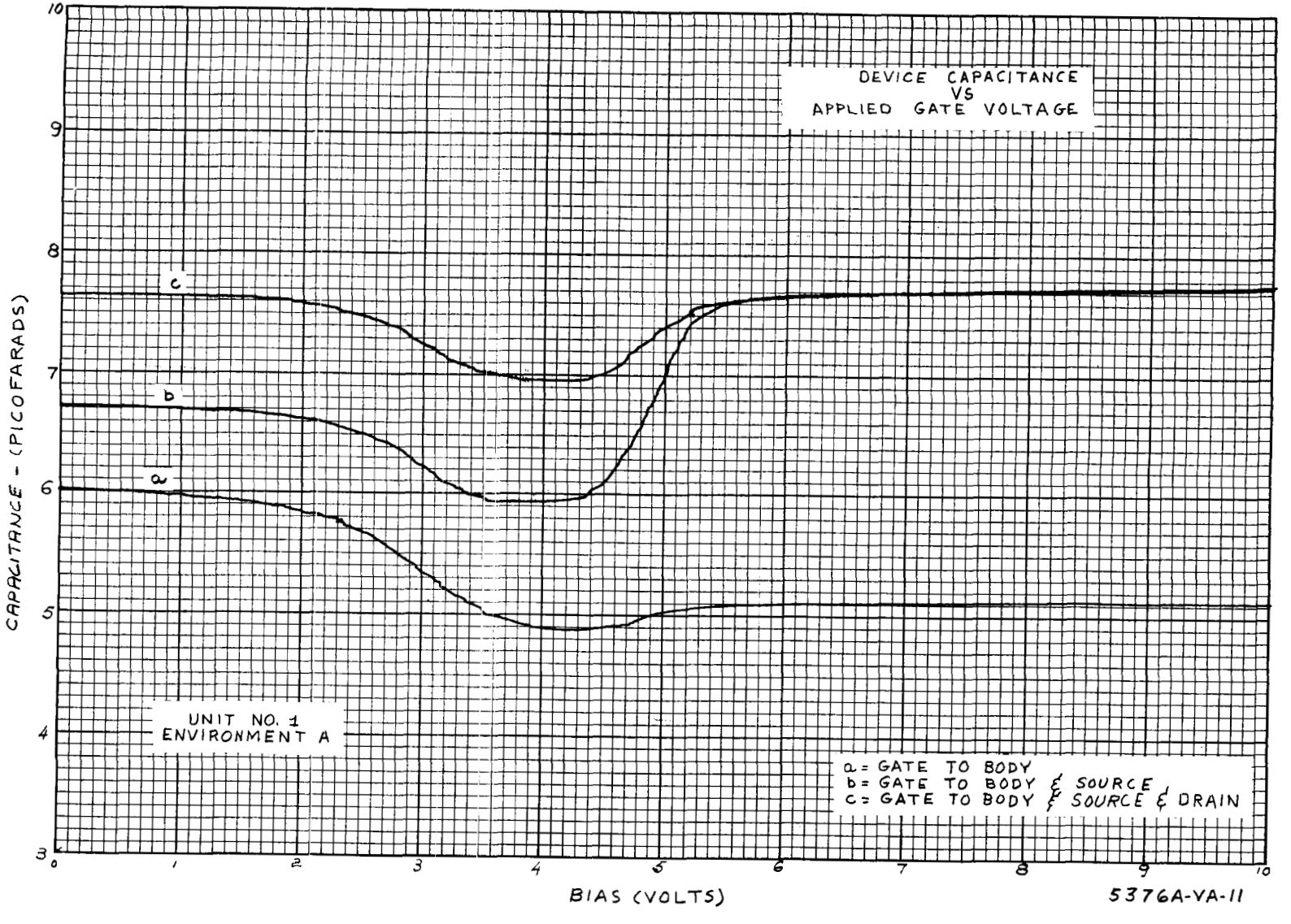


Figure 11. Voltage-Dependent Curves for Unit No. 1
Before Temperature - Bias Stress

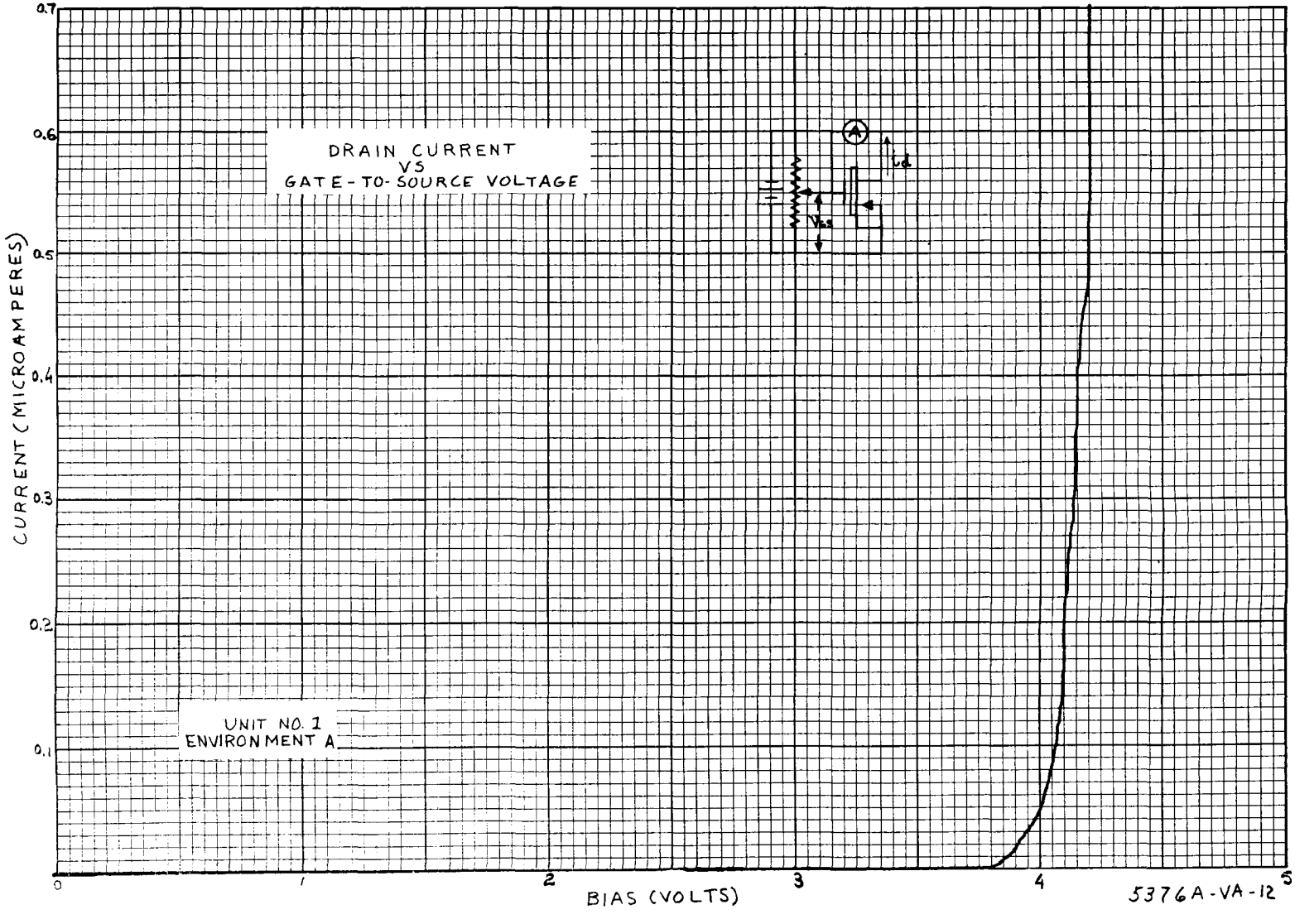


Figure 12. Conductance Characteristics of Unit No. 1
Before Temperature - Bias Stress

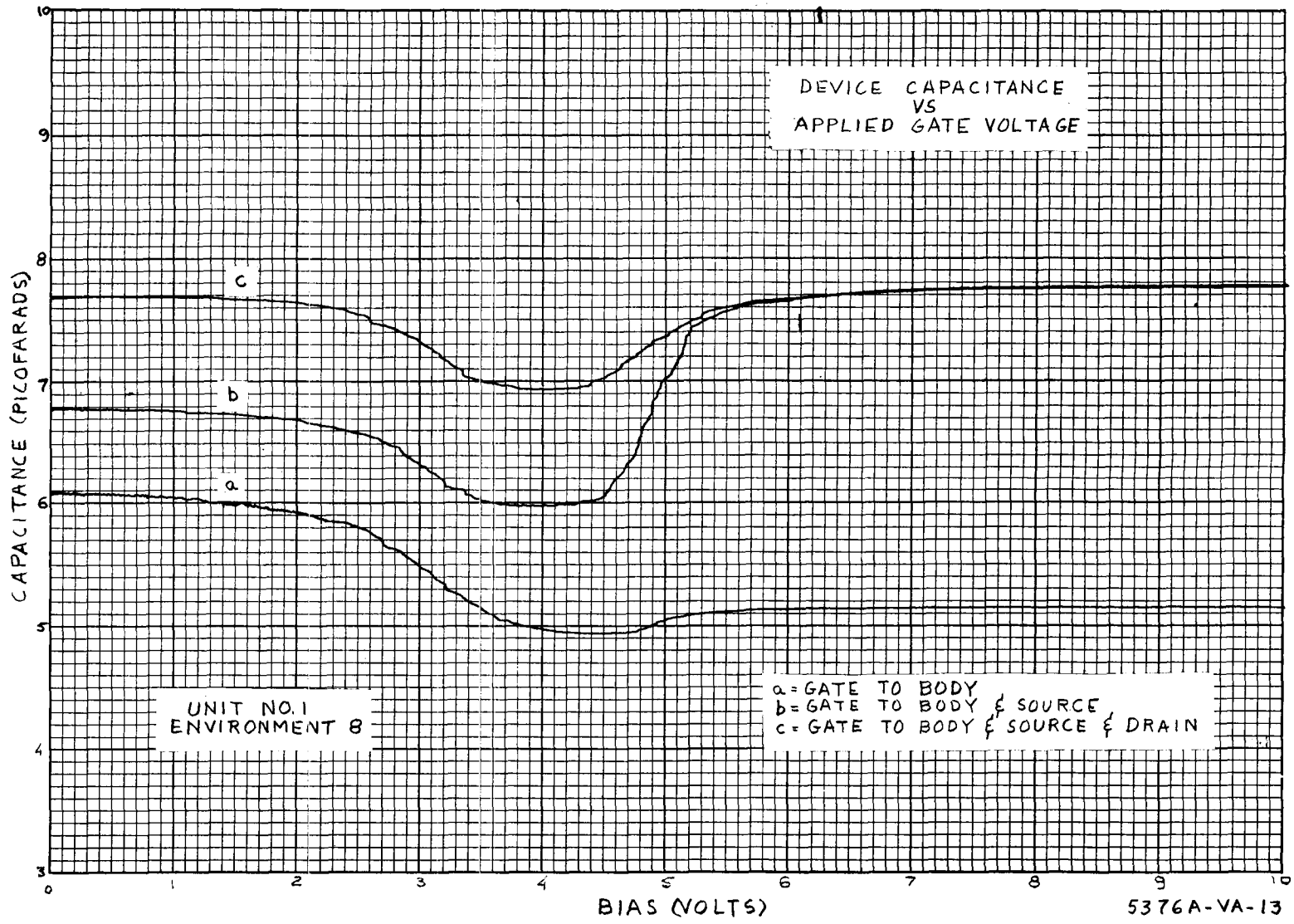


Figure 13. Voltage-Dependent Capacitance Curves for Unit No. 1 After Temperature Stress Only

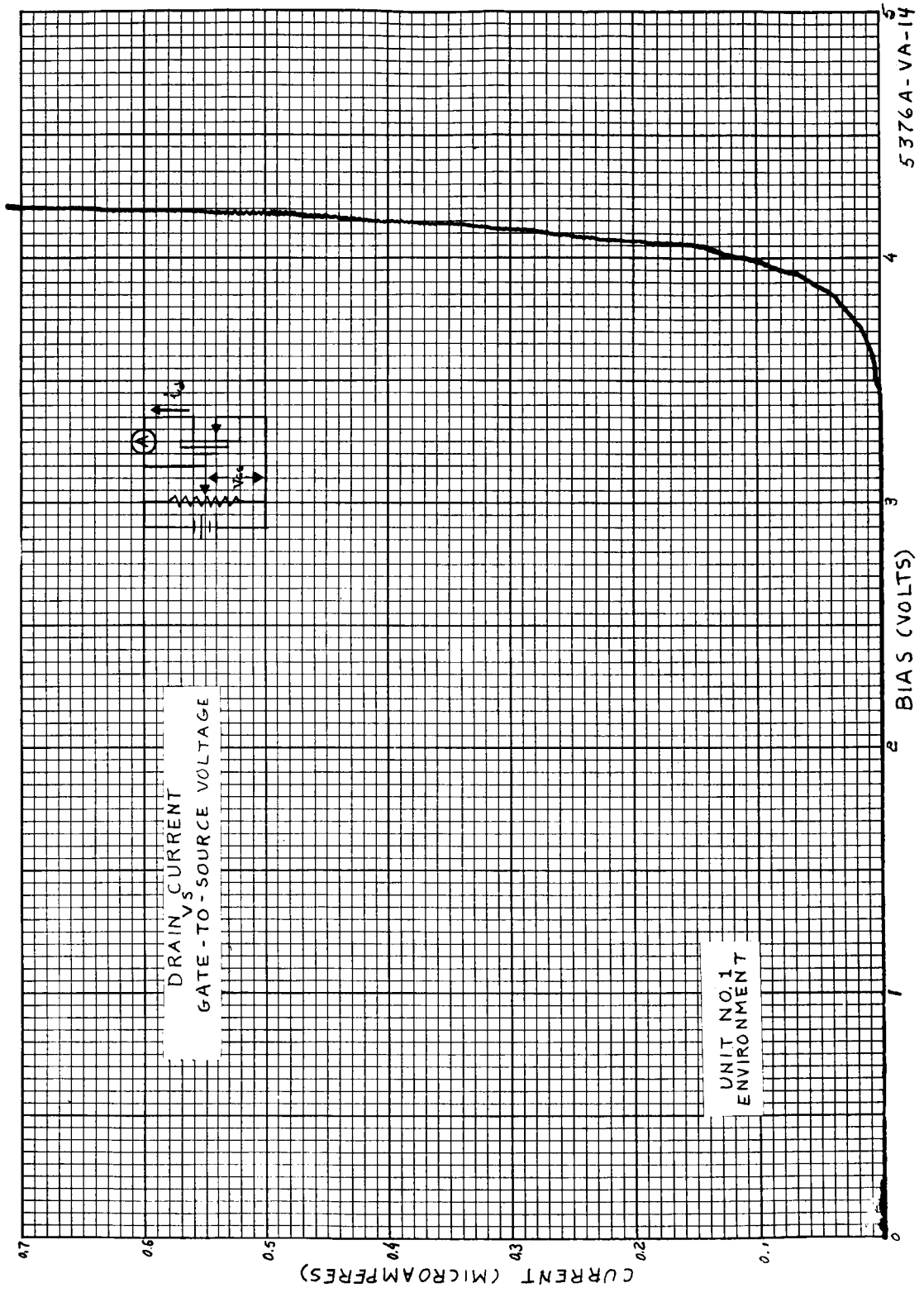


Figure 14. Conductance Characteristics of Unit No. 1
After Temperature Stress Only

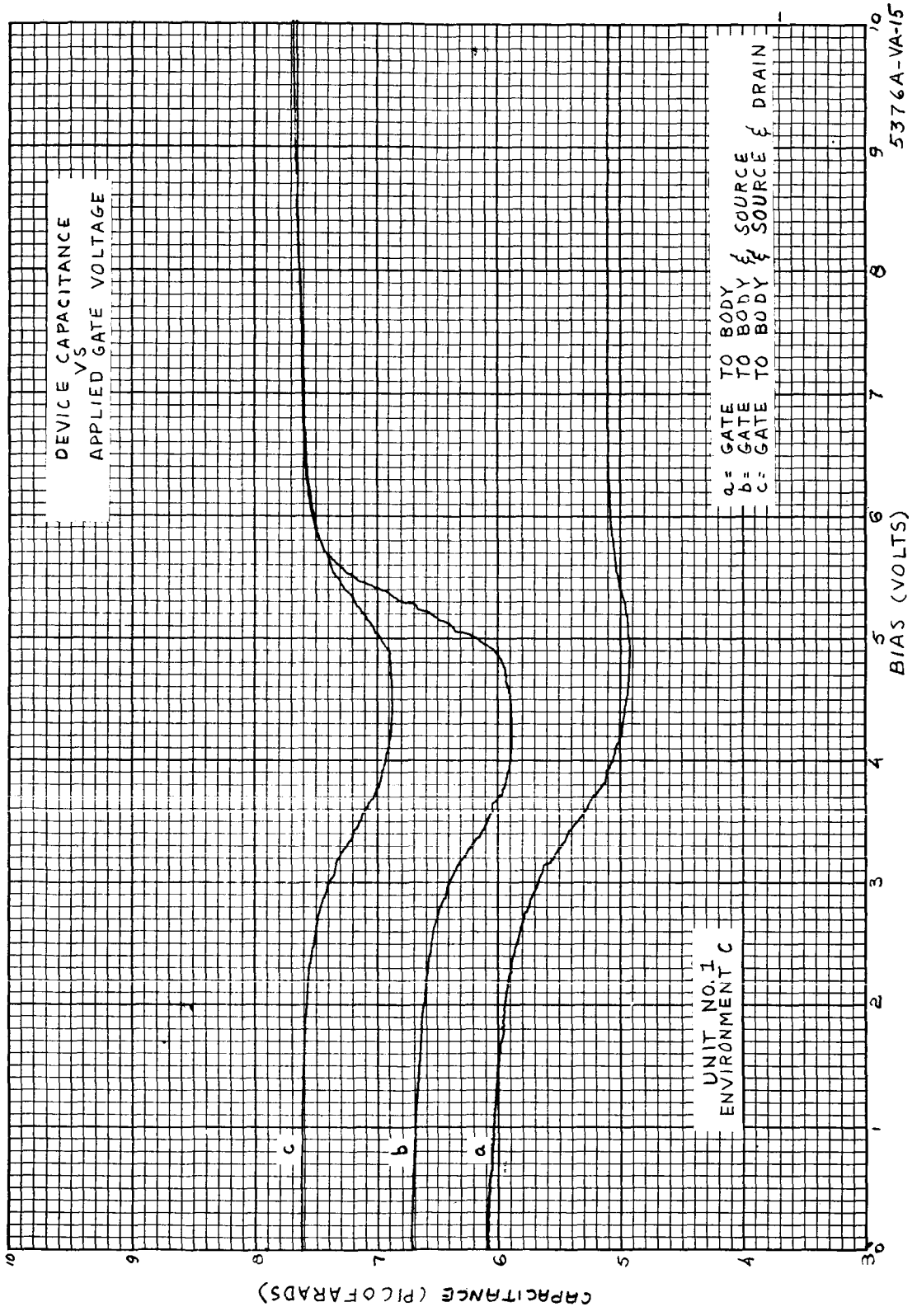


Figure 15. Voltage-Dependent Capacitance Curves for Unit No. 1
After Temperature - Bias Stress

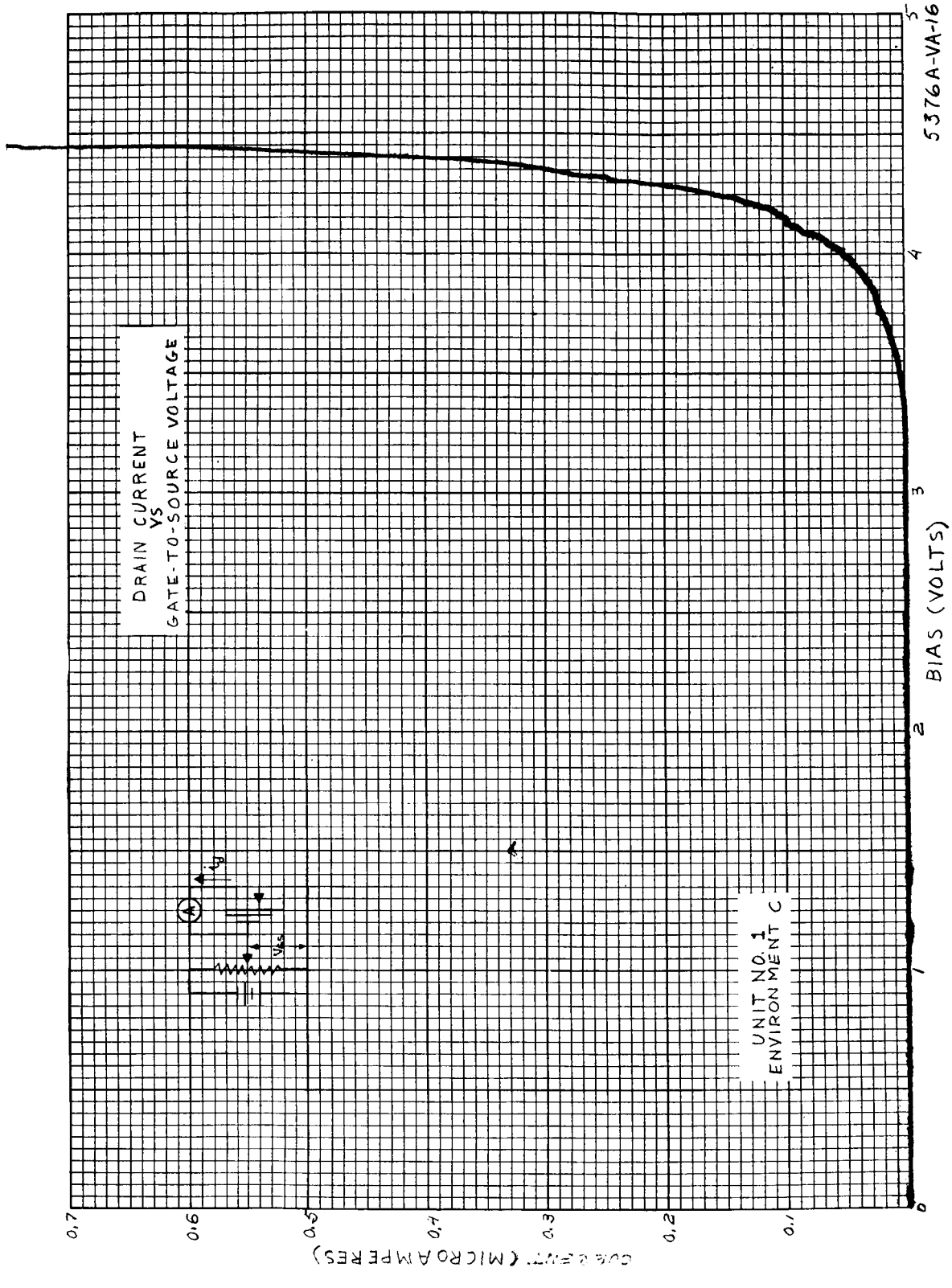


Figure 16. Conductance Characteristics of Unit No. 1 After Temperature and Bias Stress

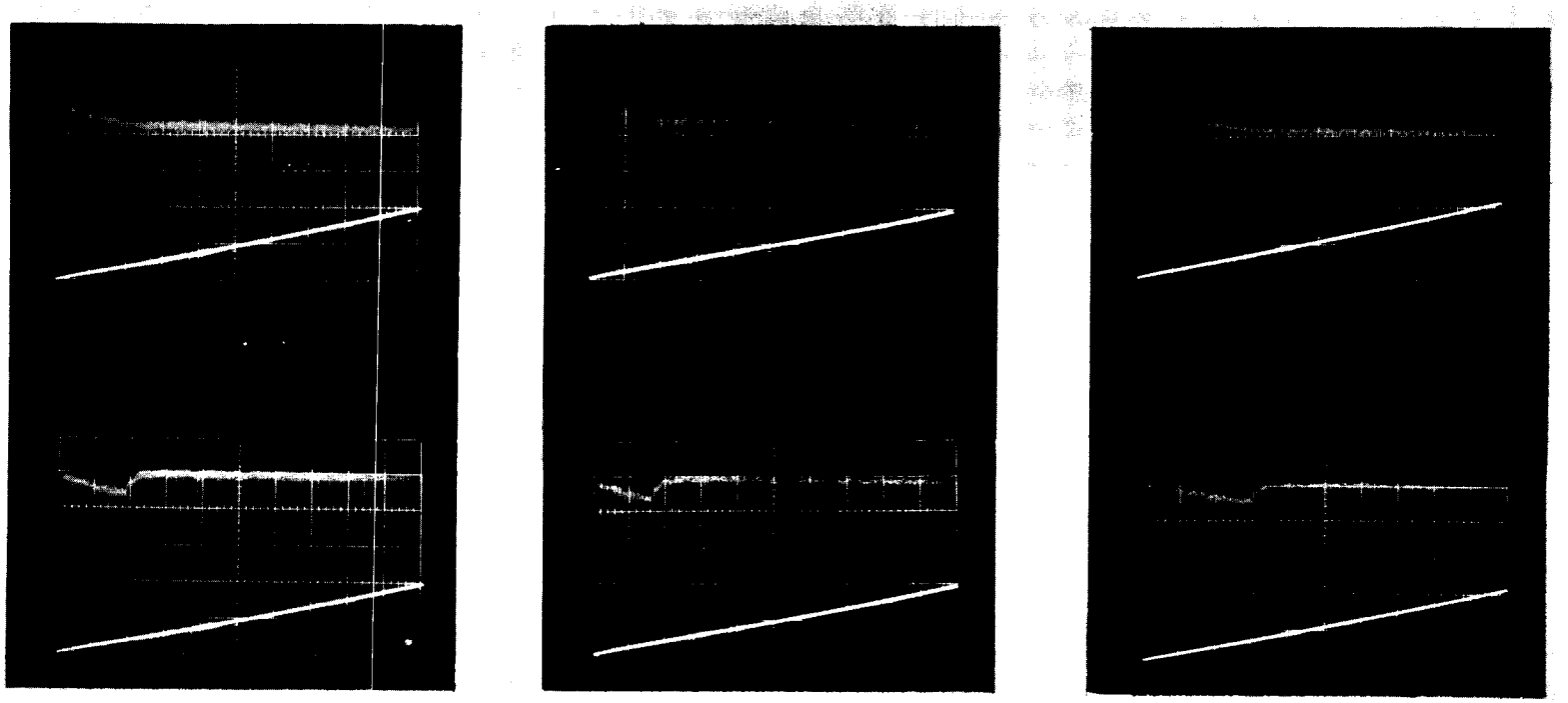


Figure 17. Voltage-Dependent Capacitance Curves for Unit No. 2 Detected by Admittance Technique

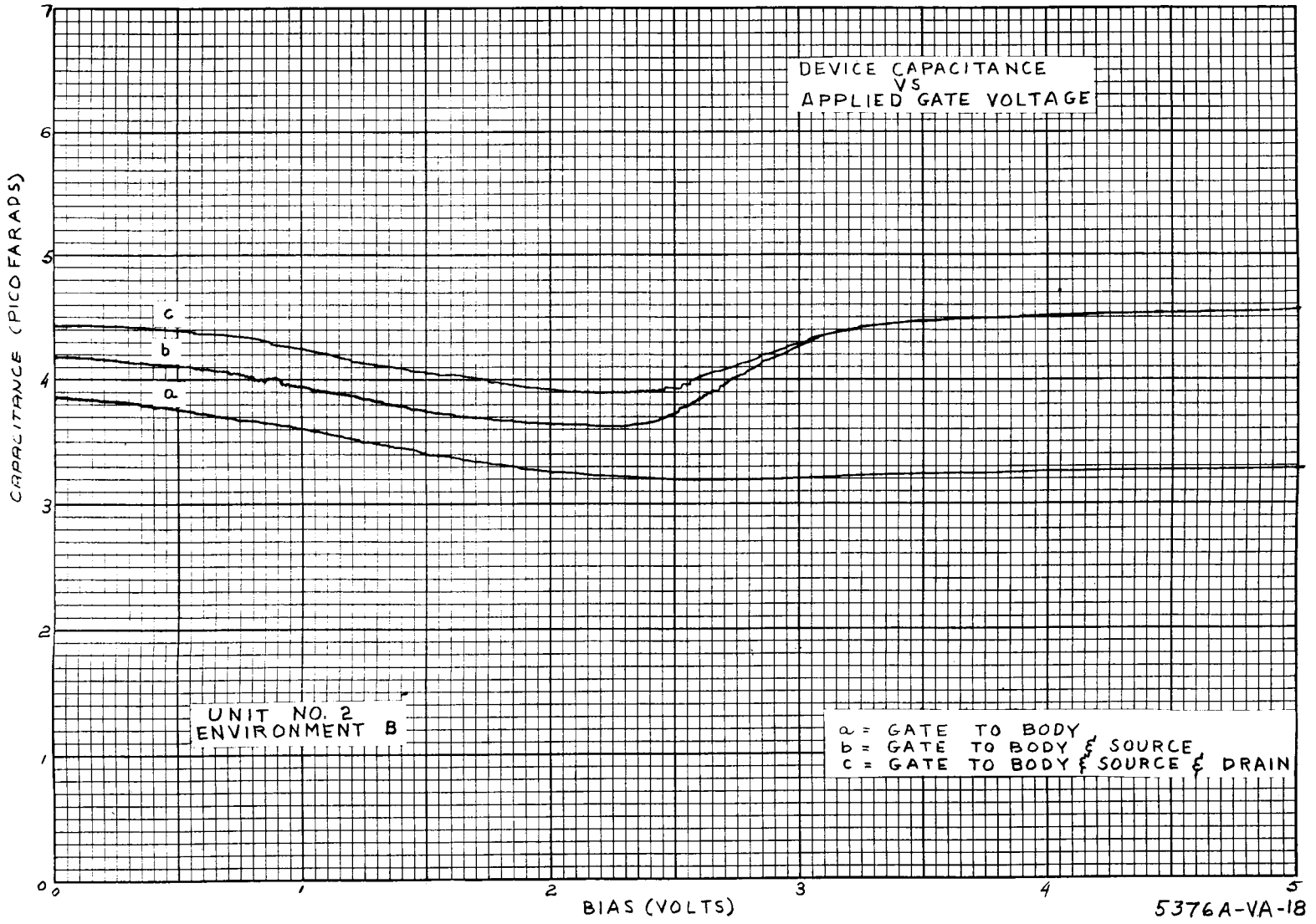


Figure 18. Voltage-Dependent Capacitance Curves for Unit No. 2 Before Temperature - Bias Stress

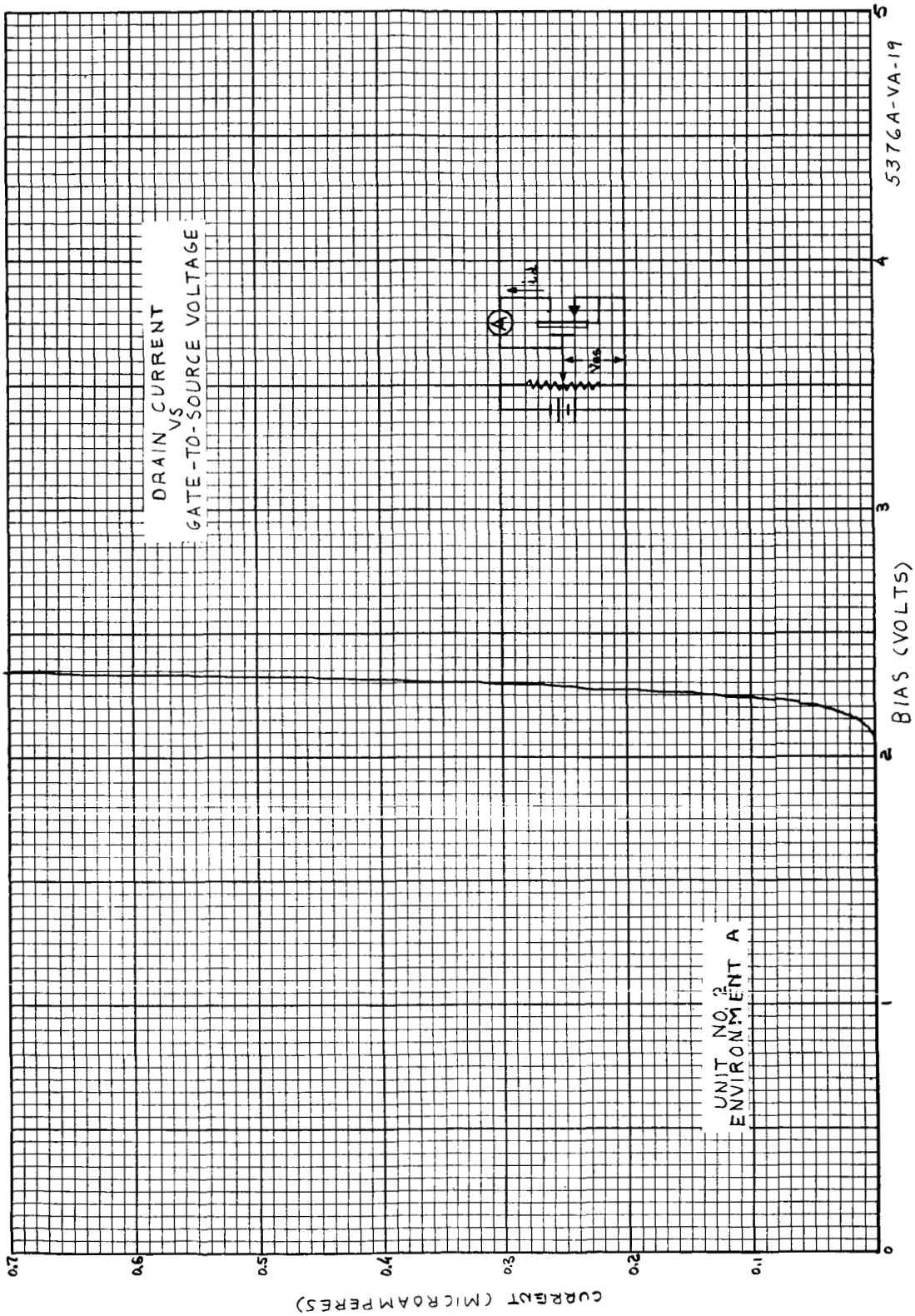


Figure 19. Conductance Characteristics of Unit No. 2
Before Temperature - Bias Stress

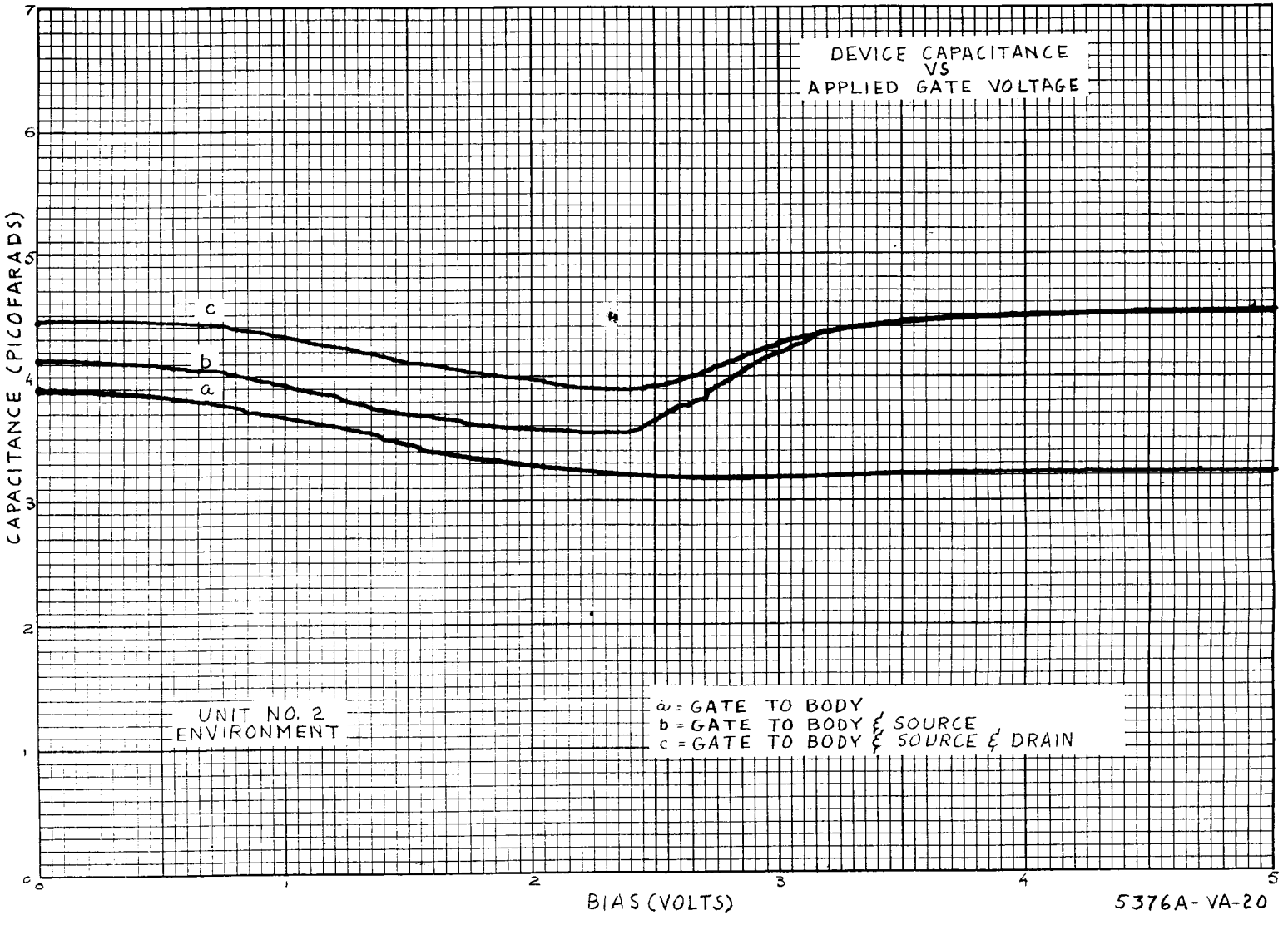


Figure 20. Voltage-Dependent Capacitance Curves for Unit No. 2 After Temperature Stress Only

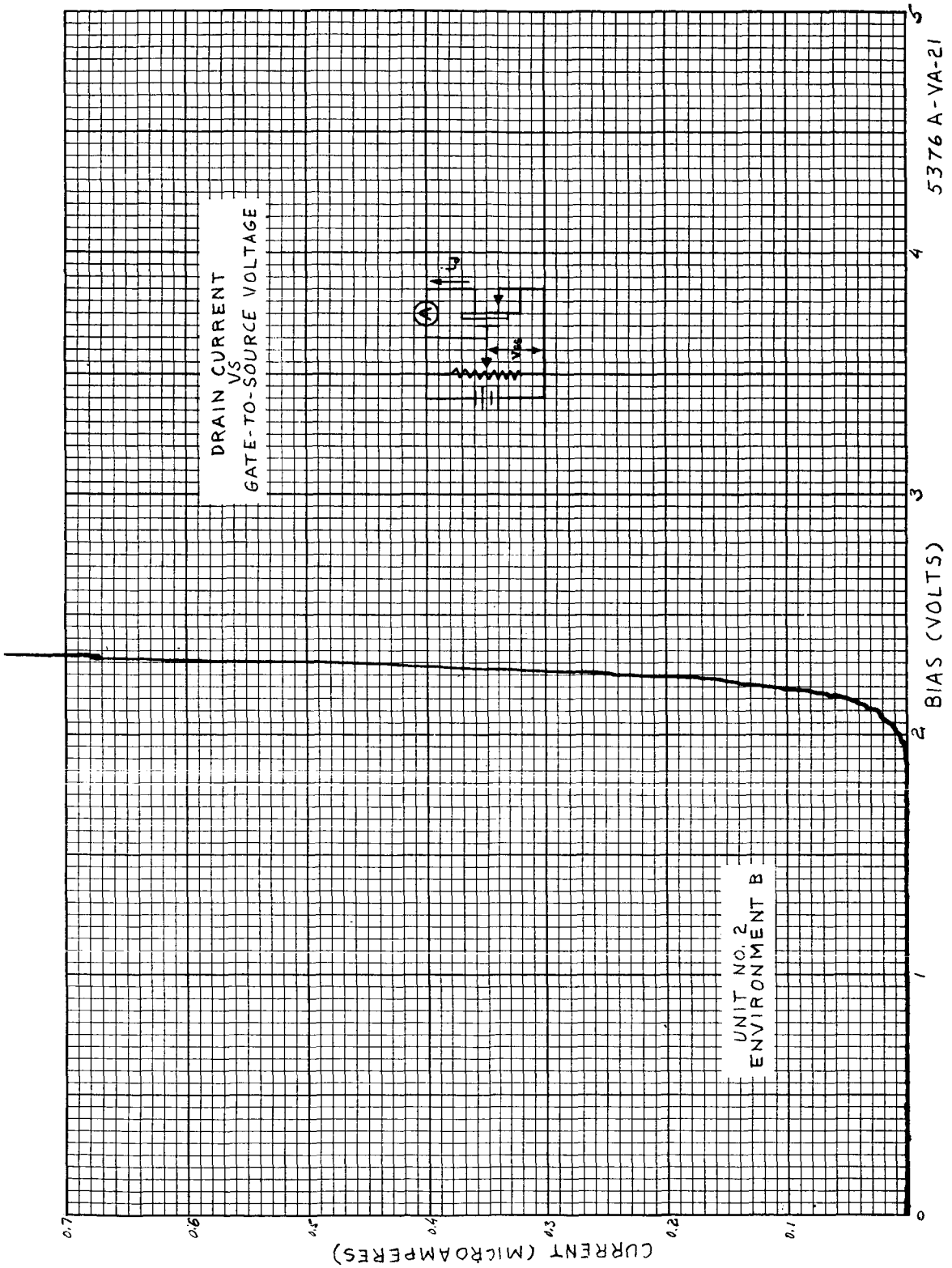


Figure 21. Conductance Characteristics of Unit No. 2 After Temperature Stress Only

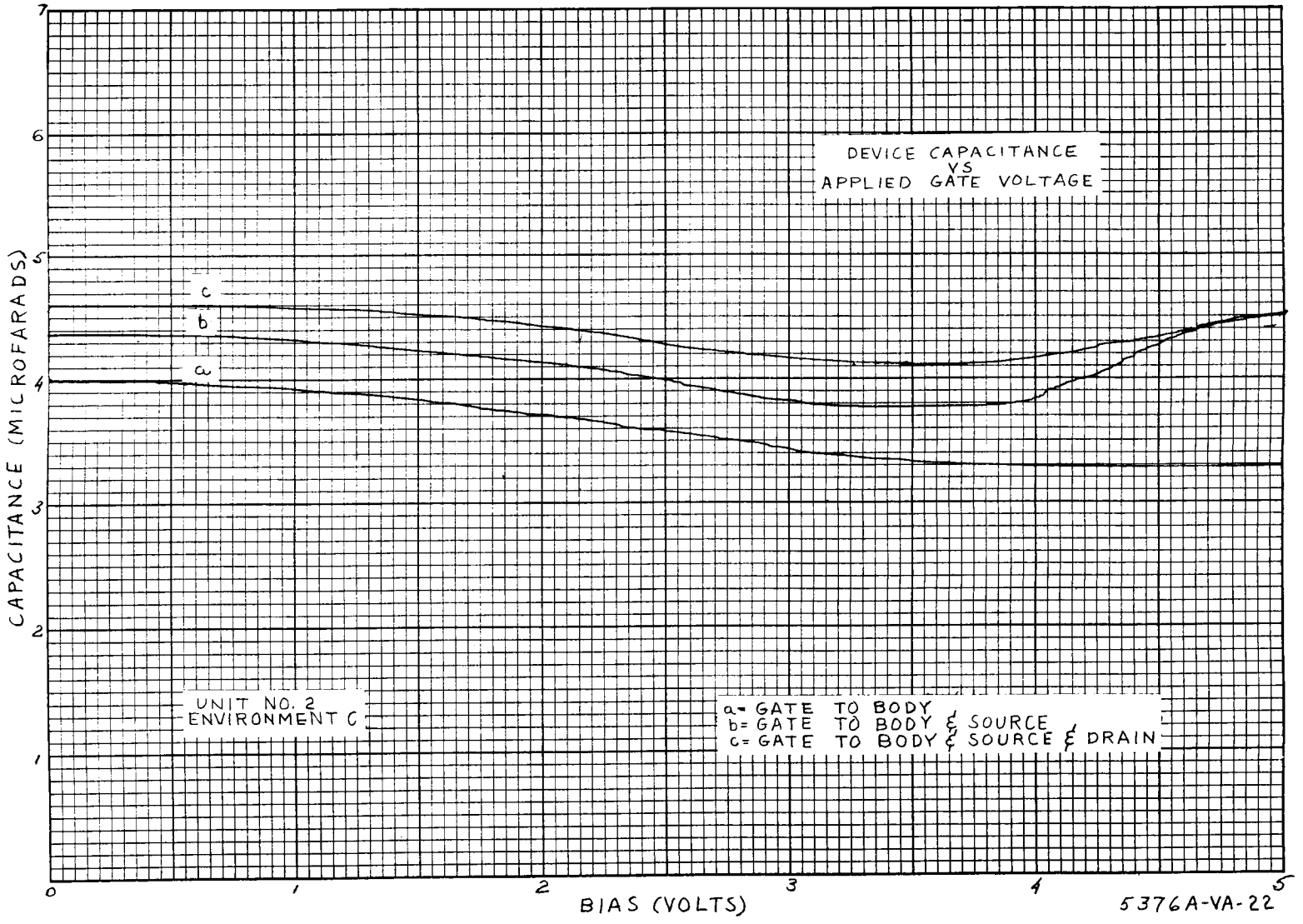


Figure 22. Voltage-Dependent Capacitance Curves for Unit No. 2 After Temperature - Bias Stress

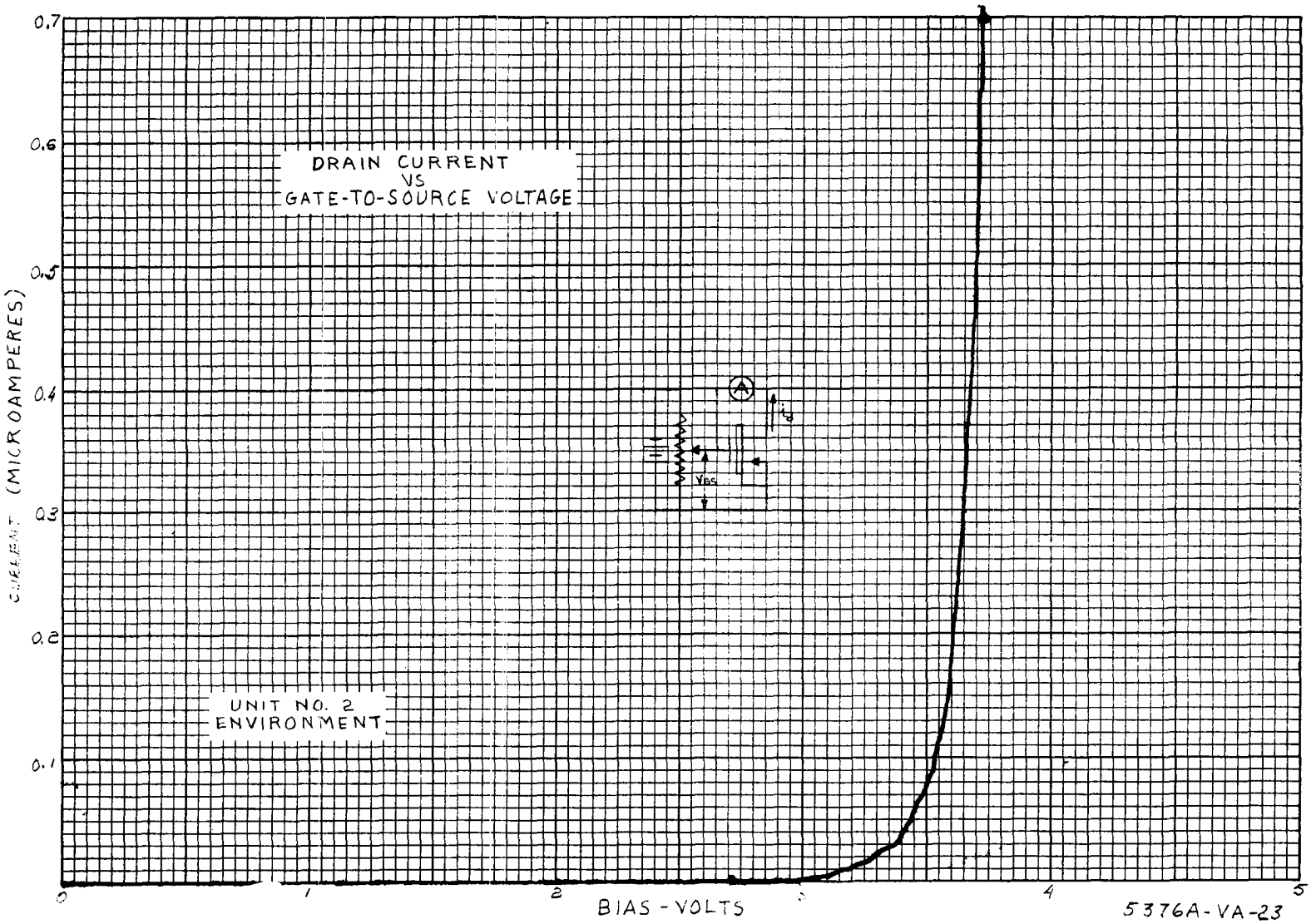
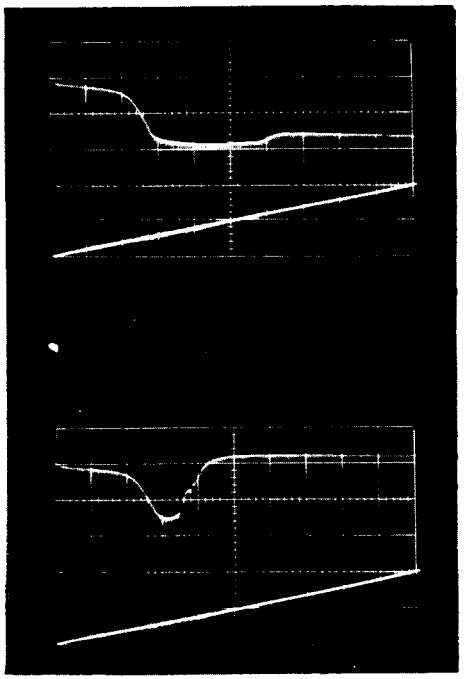
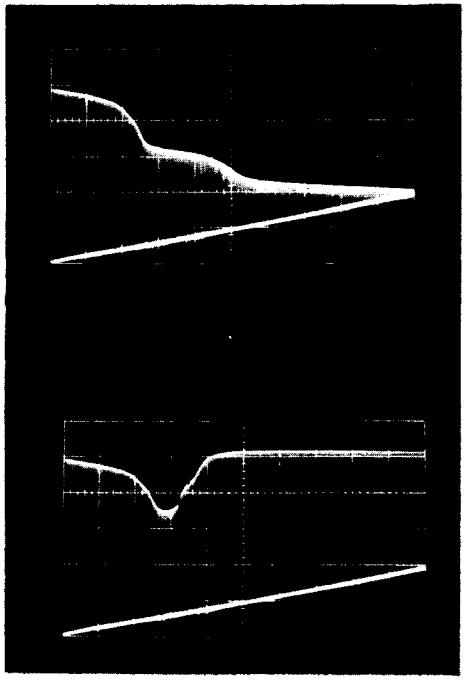


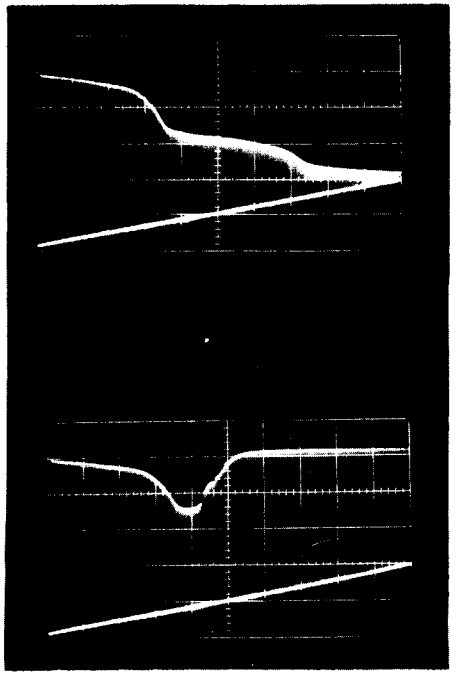
Figure 23. Conductance Characteristics of Unit No. 2
After Temperature - Bias Stress



INITIAL ROOM TEMPERATURE
CHARACTERISTICS



CHARACTERISTICS AFTER ENVIRONMENT
OF 150°C FOR 7 HOURS



CHARACTERISTICS AFTER ENVIRONMENT
OF 150°C WITH GATE VOLTAGE
OF +15V FOR 16 HOURS

(SWEEP 5 MSEC PER DIVISION)

UPPER TRACE (VERTICAL SCALE 0.5 MV PER DIVISION)
UPPER GRID: CAPACITANCE FROM GATE TO BODY
LOWER GRID: CAPACITANCE FROM GATE TO BODY TIED TO SOURCE
LOWER TRACE (VERTICAL SCALE 5V PER DIVISION)
BIAS VOLTAGE DISPLAY

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Figure 24. Voltage-Dependent Capacitance Curves for Unit No. 3 Detected by Admittance Technique

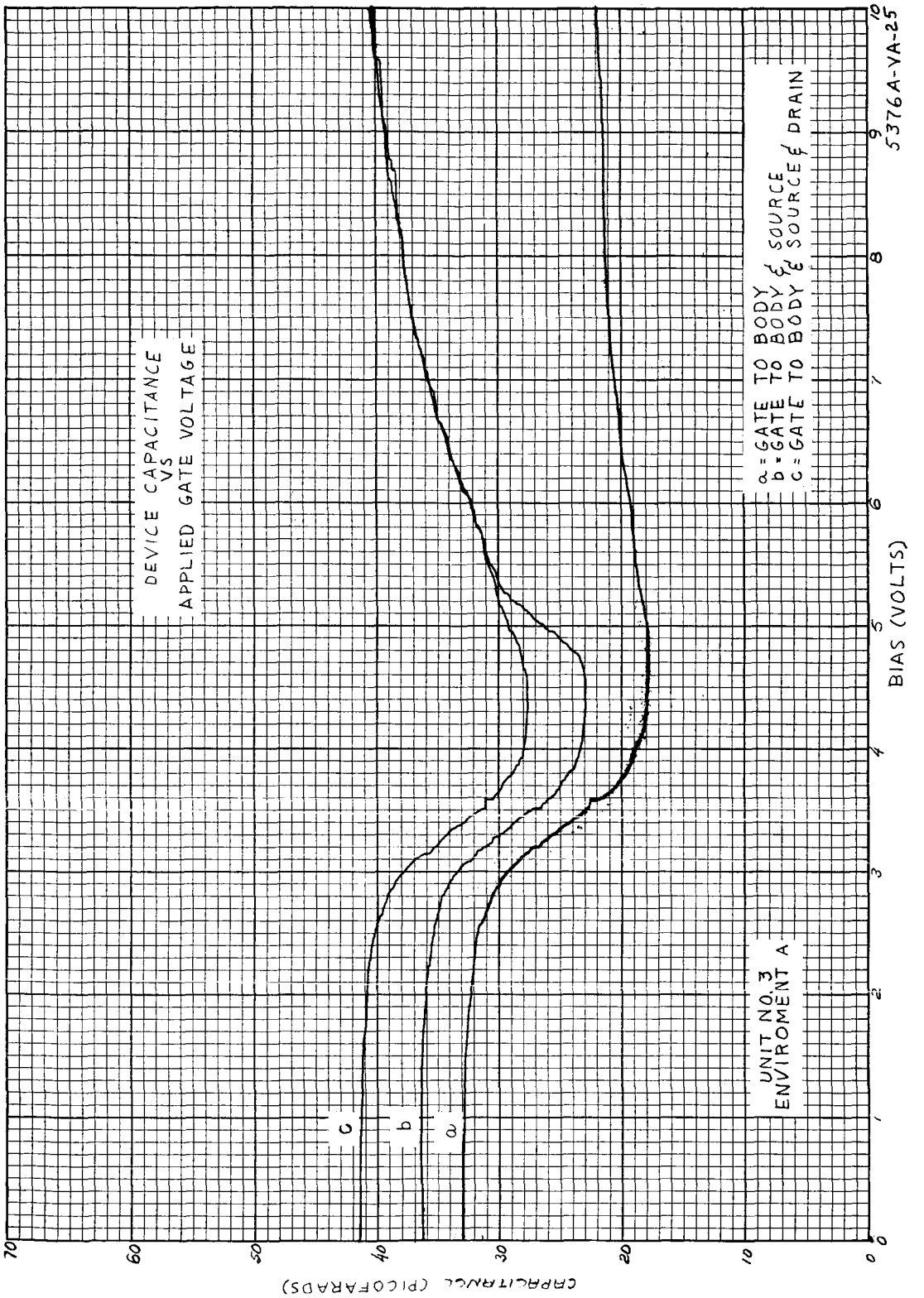

Figure 25. Voltage-Dependent Capacitance Curves for Unit No. 3
Before Temperature - Bias Stress

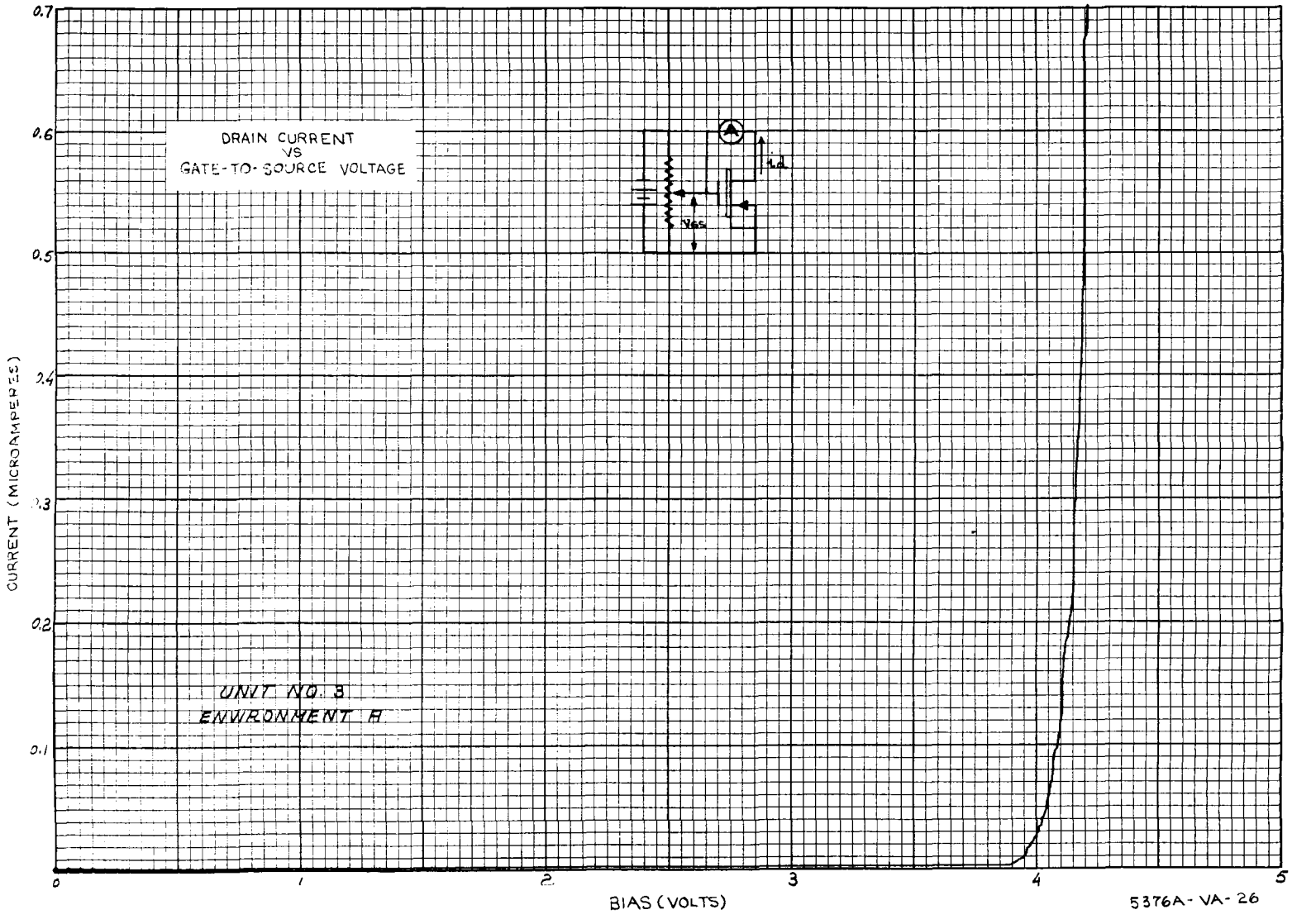

Figure 26. Conductance Characteristics of Unit No. 3
Before Temperature - Bias Stress

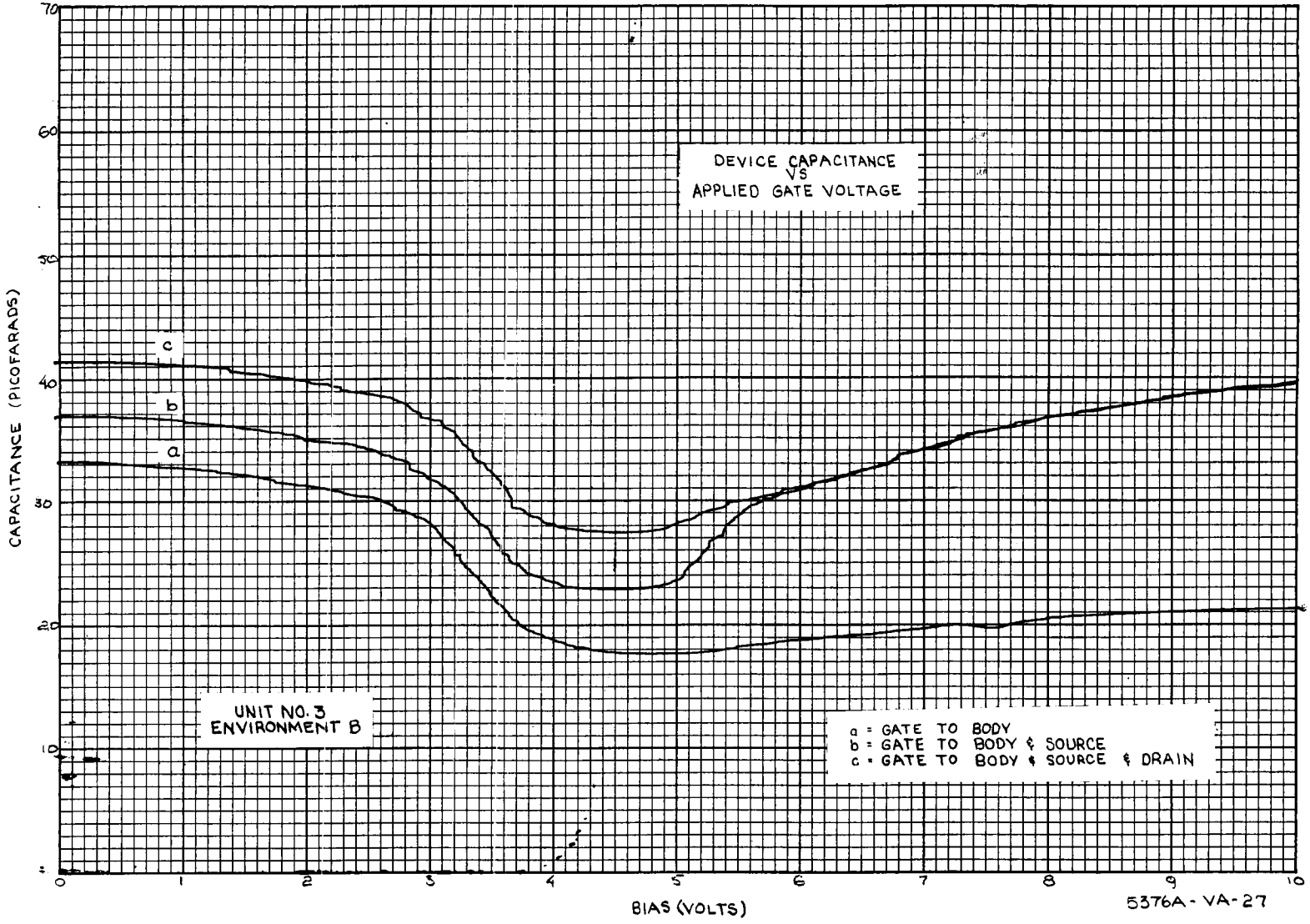

Figure 27. Voltage-Dependent Capacitance Curves for Unit No. 3 After Temperature Stress Only

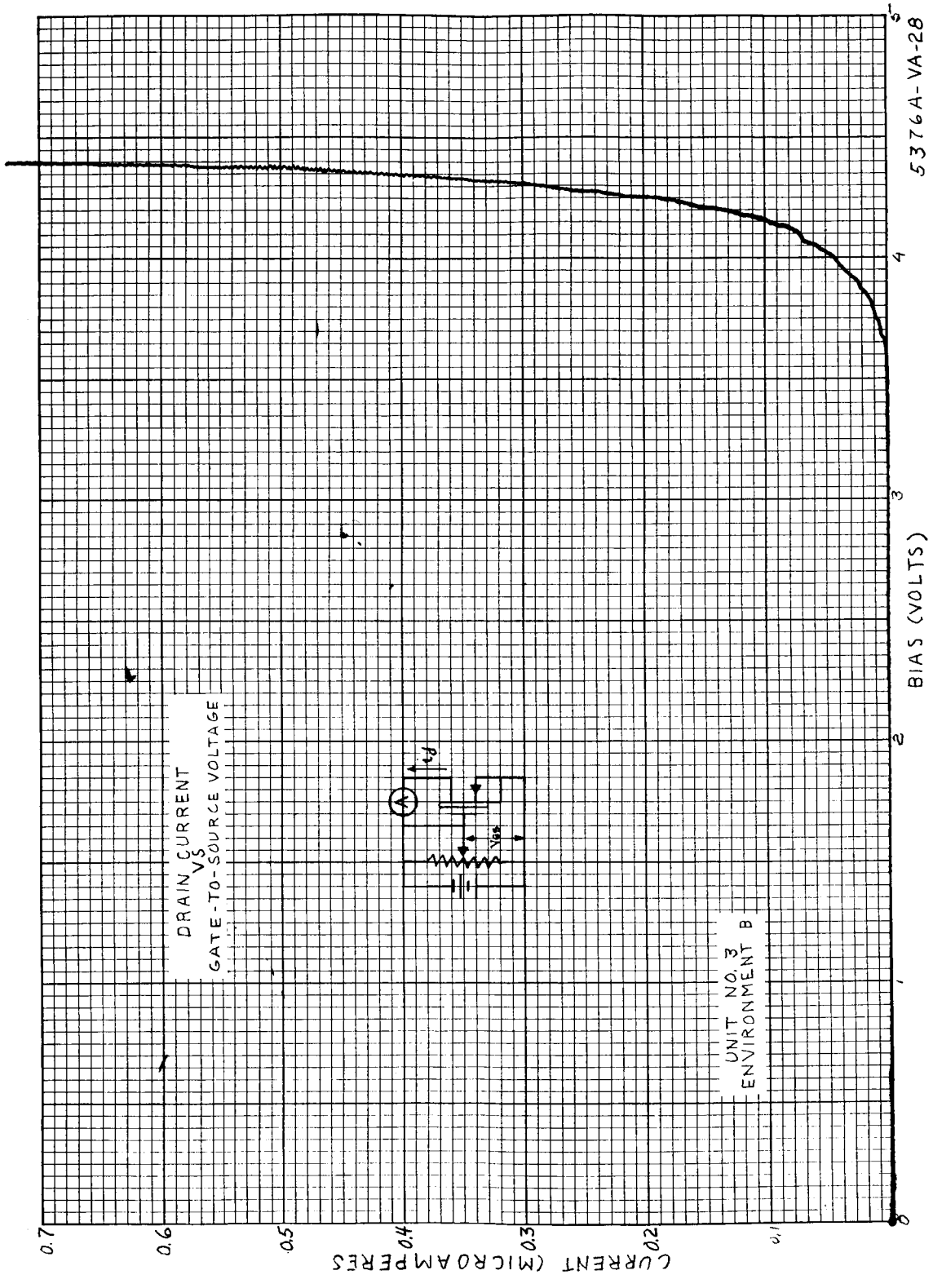

Figure 28. Conductance Characteristics of Unit No. 3
After Temperature Stress Only

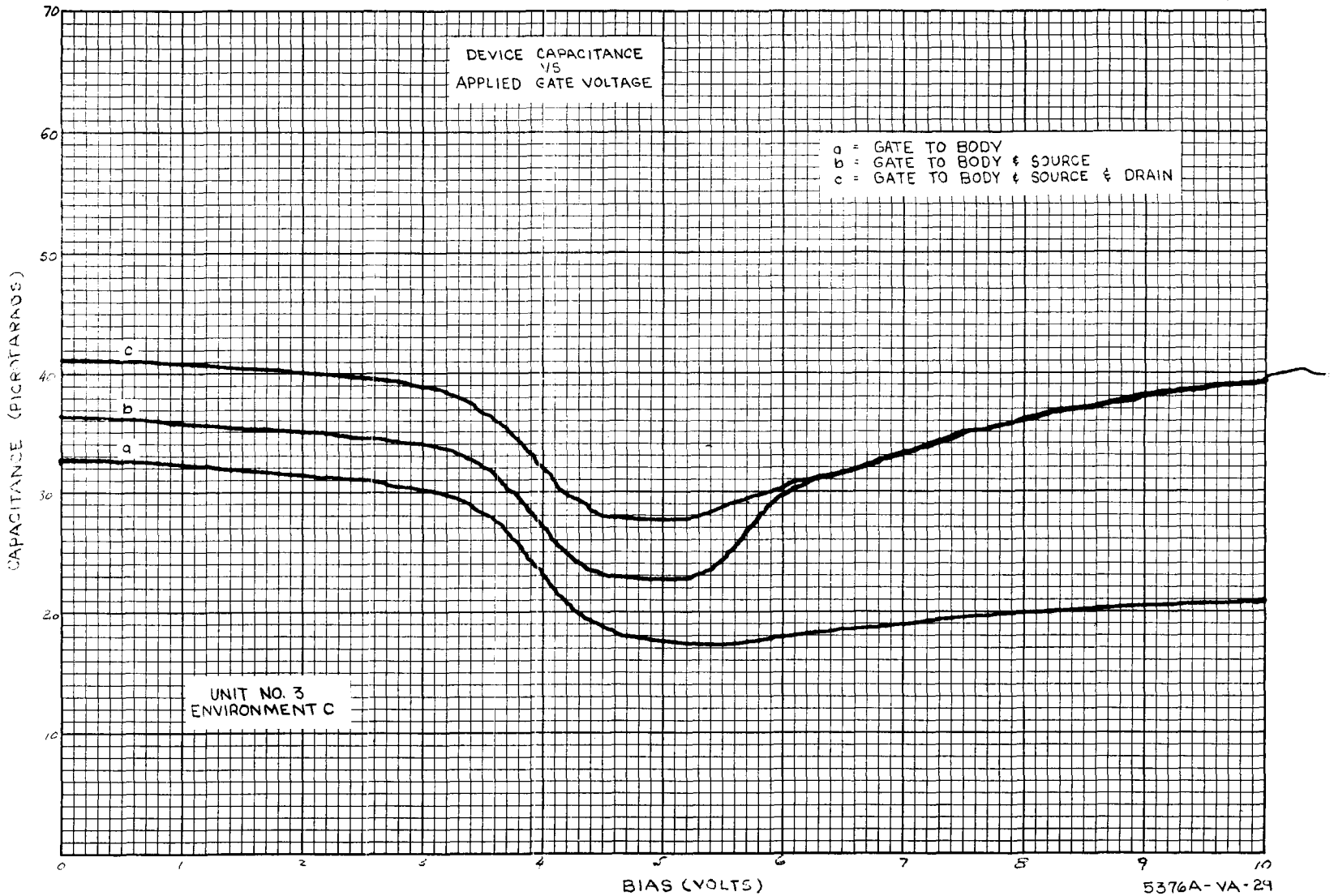

Figure 29. Voltage-Dependent Capacitance Curves for Unit No. 3 After Temperature - Bias Stress

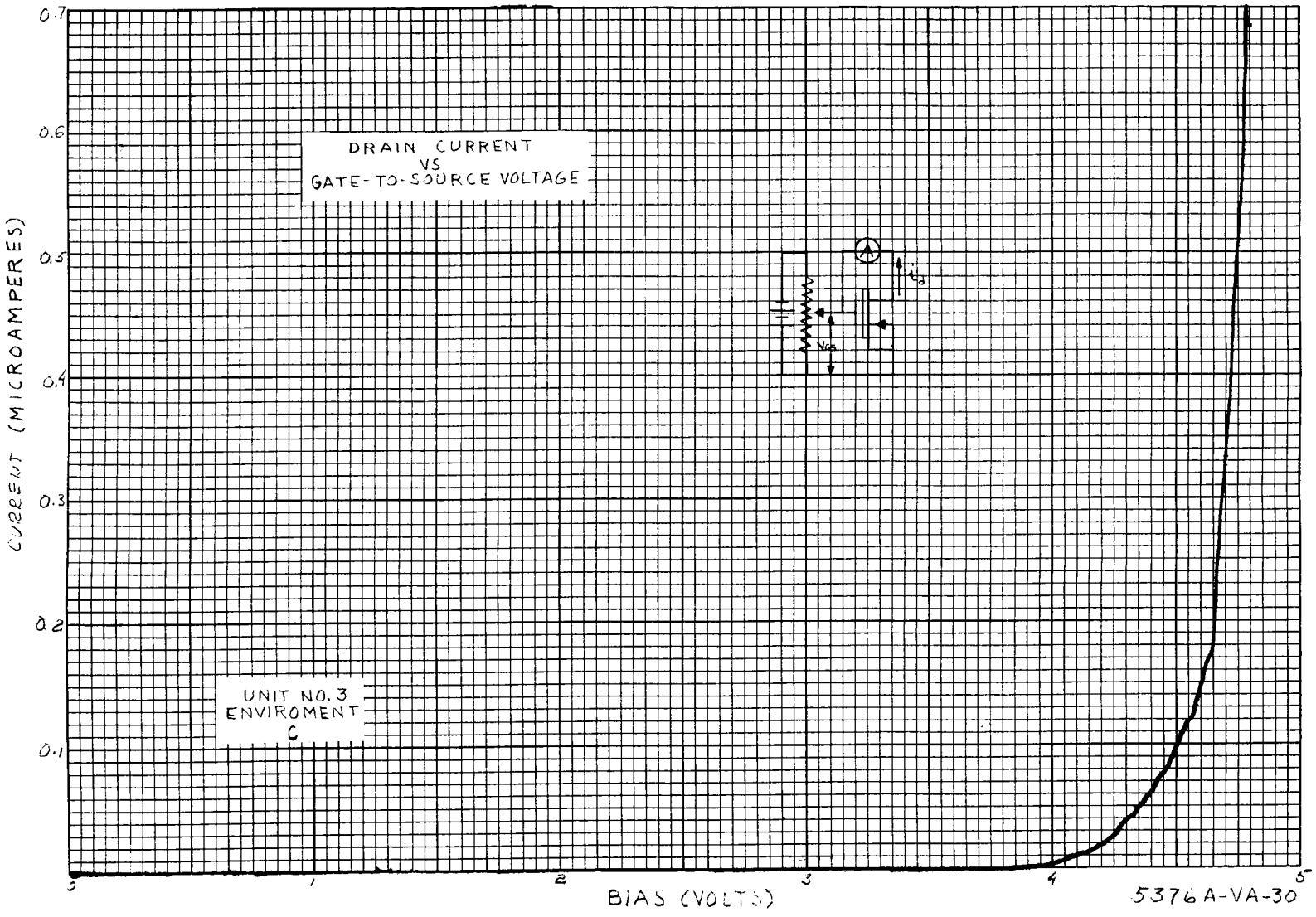

Figure 30. Conductance Characteristics of Unit No. 3 After Temperature - Bias Stress

The capacitance curves show a dependency on the manner in which the terminals were connected. Specifically, when the source or the source and drain were connected to the body of the device, the data indicates not only the presence of the inversion charges at the higher voltages but also a marked increase in the capacitance for the lower voltage range. Also, the capacitance exhibited in this lower range is always greater if both the source and drain are connected to the body. This extra capacitance is due to the fact that the metal-oxide sandwich overlaps onto the source and drain regions. This overlap constitutes a capacitance which is added in parallel with the gate capacitance when the source or drain terminals are connected to the body. The amount of increase to be expected in these situtations depends not only on the design of the unit but also on the degree of accuracy in the mask alignment during processing.

The changes in characteristics exhibited by the three units are summarized in tables 1 and 2.

TABLE 1

VARIATION SUBSEQUENT TO THE CONDITIONS OF ENVIRONMENT B (VOLTS)

Unit No.	1	2	3
Q_{ss}/C_o	+0.1	<0.05	<0.05
V_T	-0.15	-0.1	+0.1

TABLE 2

VARIATION SUBSEQUENT TO THE CONDITIONS OF ENVIRONMENT C (VOLTS)

Unit No.	1	2	3
Q_{ss}/C_o	+0.3	+1.05	+0.4
V_T	+0.2	+1.30	+0.8

The notation Q_{ss}/C_o refers to the displacement in the capacitance characteristics, and V_T refers to the change in the turn-on voltage. The signs refer to an increase or decrease in the voltage magnitudes and do not imply a referenced bias direction. The turn-on voltage was chosen as the point where the device is passing 0.1 microampere of current through the drain terminal. The configuration used to measure this turn-on voltage is shown on the conductance graphs. A voltage increase is taken to be a sign of instability, since decreasing voltages are more likely to be caused by incomplete processing.

According to data given in tables 1 and 2 above, unit No. 1 exhibited the greatest stability and unit No. 2 was the least stable. There is a marked correlation between instability and the change in surface state charge concentration. This is especially evident in the results obtained after subjecting the units to both a temperature and reverse bias stress. These results then tend to substantiate the oxide vacancy - ion migration models proposed to explain MOS instability.

The data recorded for unit No. 3 points out the special character of the testing techniques. The capacitance curves obtained through the admittance method exhibit a second plateau, whereas those obtained by the frequency-detection technique do not. This phenomenon is most likely associated with the conductive properties of the device and are most readily explained by charge traps in the oxide. In this regard, at the voltage corresponding to the start of the second plateau, a sufficient number of the oxide traps are activiated to render a considerable portion of the inversion charges immobile. This would cause a decrease in the capacitance display as determined by the admittance method but would not necessarily affect the capacitance as determined by the frequency detection technique. This dual response is due to the following consideration. The traps tend to immobilize a considerable portion of the surface charge; this decrease is reflected as a decrease in the admittance of the device. However, the immobilization of these charges does not in effect remove this charge from the vicinity of the surface. Therefore the capacitance of the device will not exhibit the effects of this immobilization.

It has been reported[4] that the effect of oxide traps is dependent upon their distance from the silicon surface and upon the magnitude of the applied voltage. The large magnitude of capacitance associated with unit No. 3 indicates that it has a small oxide layer. The unit would therefore be all the more susceptible to the existence of oxide traps. Both this fact and the strong voltage-dependent nature of the observed plateau tend to support the existence of oxide traps in this unit. Moreover, the results of the environmental tests indicate that these traps are mobile under stress of temperature or temperature and bias. It should be noted that after the device was subjected to the temperature and bias environment, the plateau shifted to a high voltage - as is expected for the reverse bias. Also, the existence of these oxide traps may be responsible to some degree for the instability exhibited by this unit, because the mechanisms involved with oxide traps are very similar to those for oxide vacancies.

4. E. P. Heisman and G. Warfield, "The Effects of Oxide Traps on the MOS Capacitance," IEEE Transactions on Electron Devices, (April 1965).

4. CONCLUSIONS AND SUMMARY

The salient information pertinent to the study of stability in MOS structures was effectively monitored through the combined use of the two complementary capacitance-voltage measuring techniques.

Performance indicates that the voltage-dependent capacitance curves provide a good insight into the physical and operational nature of the MOS unit and also reveal any instability associated with these devices. Although the data indicate that instability is associated with the redistribution of charge in the oxide, it has not been possible to differentiate conclusively between the oxide vacancy[5] and the ion mobility models.[6] The complementary nature of these two models indicates the need for further study under stringently controlled processing procedures. Collateral study into the effects of different material concentrations and oxide thicknesses would also prove beneficial in gaining a more thorough understanding of the various electro-physical mechanisms involved in MOS device operations. In this regard, both for the correlation of the device to a circuit model and in the study of device stability, the use of the voltage-dependent capacitance curves serves as an important analytical tool.

5. D. R. Kerr, "Effect of Temperature and Bias on Glass-Silicon Interfaces," IBM Journal of Research and Development, Vol. 8, No. 4 (September 1964).

   D. P. Seraphim, et al, "Electrochemical Phenomena in Thin Films of Silicon Dioxide on Silicon," IBM Journal of Research and Development, Vol. 8, No. 4 (September 1964).

6. S. R. Hofstrin and B. P. Heiman, "The Silicon Insulated Gate Field Effect Transistor," IEEE Proceedings, (September 1963).

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